



深圳市一众显示科技有限公司

SHEN ZHEN TEAM SOURCE DISPLAY TECH. CO., LTD

TFT-LCD Module Specification

Module NO.: TST030GN06-01**Version: V1.0**☐ APPROVAL FOR SPECIFICATION☐ APPROVAL FOR SAMPLE**For Customer' s Acceptance:**

Approved by	Comment

Team Source Display:

Presented by	Reviewed by	Approved by
HCR		

2. RECORD OF REVISION

Rev	Date	Item	Page	Comment	Source
1	09/MAR/21'	All	All	Initial Preliminary	

3. GENERAL SPECIFICATIONS

Parameter	Specifications	Unit
Screen Size	3.0 (Diameter)	inch
Display Format	432(H) x (R,G,B) x 432(V)	dot
Active Area	74.3904(H) x 74.3904(V)	mm
Pixel Pitch	0.1722(H) x 0.1722(V)	mm
Pixel Configuration	Stripe	
Outline Dimension	84.2(H) x 89.2(V) x 6.38(D)	mm
Back-light	LED	
TFT-LCD Display mode	Normally Black	
Weight	50	g
View Angle direction(TFT)	All	
IC Part Number	HX8363-A	
Our components and processes are compliant to RoHS & REACH & Halogen Free standard		

4. ABSOLUTE MAXIMUM RATINGS

Ta=25°C

Parameter	Symbol	Min.	Max.	Unit	Remark
Power supply voltage	VDD	0.3	4.6	V	
	VDDI	0.3	4.6	V	
Operating temperature	Top	-30	85	°C	
Storage temperature	Tst	-30	85	°C	

5. ELECTRICAL CHARACTERISTICS

5.1 Operating Conditions

GND=0V, Ta=25°C

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remark
Power Supply voltage	VDD	2.5	-	3.3	V	
	VDDI	1.65	-	3.3	V	
Power Supply current	IVDD	-	8	-	mA	VDD=3.3V
	IVDDI	-	0.4	-	mA	VDDI=3.3V
"H" level logical input voltage	V _{IH}	0.7VDD	-	VDD	V	
"L" level logical input voltage	V _{IL}	-	-	0.3VDD	V	

5.2 Backlight Driving Consumption

Ta= 25°C

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remark
LED voltage	V _F	-	-	19.8	V	
LED current	I _F	-	60	-	mA	
LED dice Life Time		-	50,000	-	hr	



V_F : 19.8V Max.
I_F : 60mA

6. INPUT SIGNAL TIMING

6.1 AC Characteristics

Serial interface characteristic

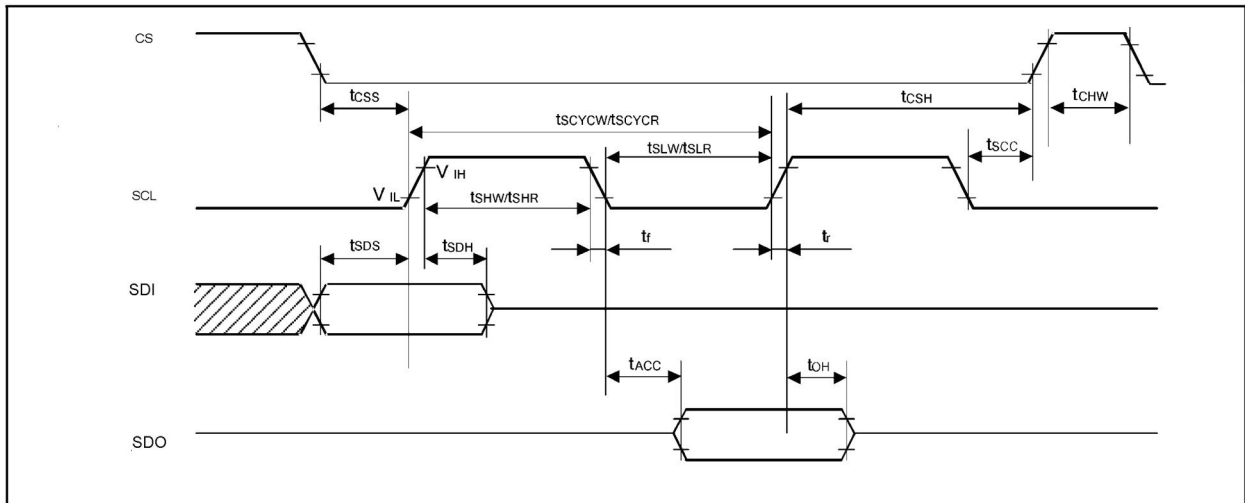


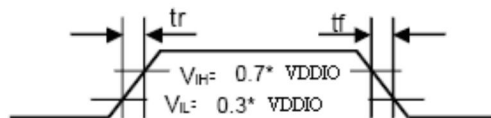
Figure 6.1-1 Serial Interface Characteristics

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Serial clock cycle (Write)	tSCYW	SCL	80			ns
SCL "H" pulse width (Write)	tSHW		30		--	
SCL "L" pulse width (Write)	tSLW		30			
Data setup time (Write)	tSDS	SDI	10			ns
Data hold time (Write)	tSDH		10		--	
Serial clock cycle (Read)	tSCYCR	SCL	150			ns
SCL "H" pulse width (Read)	tSHR		60		--	
SCL "L" pulse width (Read)	tSLR		60			
Access time	tACC	SDO For maximum CL=30pF For maximum CL=8pF	10		60	ns
Output disable time	toH	SDO For maximum CL=30pF For maximum CL=8pF	15		100	ns
SCL to Chip select	tSCC	CS	30		--	ns
CS "H" pulse width	tCHW	CS	60		--	ns
CS -SCL time (write)	tCSS	CS	30			ns
CS -SCL time (write)	tCSH		30		--	
CS -SCL time (Read)	tCSS	CS	60			ns
CS -SCL time (Read)	tCSH		65		--	

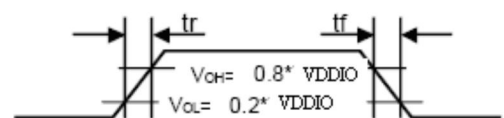
Note: The input signal rise time and fall time (tr, tf) is specified at 15 ns or less.

Logic high and low levels are specified as 30% and 70% of VDDIO for Input signals.

Input Signal Slope



Output Signal Slope



6.2 RGB interface characteristic

Vertical Timings for RGB I/F

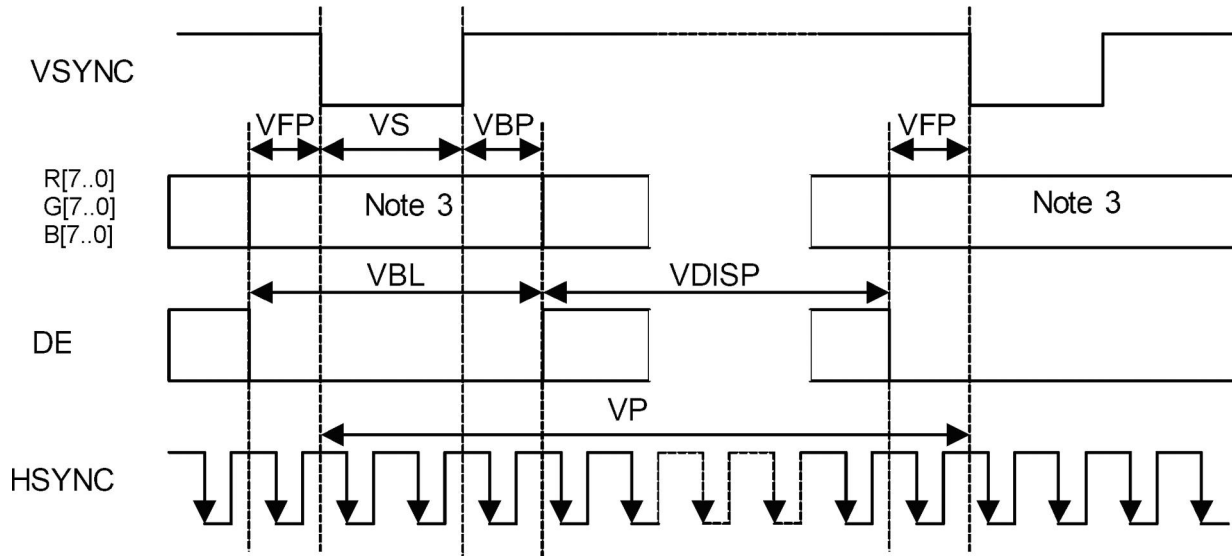


Figure 6.2-1 Vertical Timings for RGB I/F

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Vertical cycle	VP	-	646	-	650	Line
Vertical low pulse width	VS	-	2	-	4	Line
Vertical front porch	VFP	-	2	-	4	Line
Vertical back porch	VBP	-	2	-	4	Line
Vertical data start point	-	VS+VBP	4	-	8	Line
Vertical blanking period	VBL	VS+VBP+VFP	6	-	10	Line
Vertical active area	-	VDISP	-	640	-	Line
Vertical Refresh rate	VRR	-	50	-	70	Hz

Note: (1) Signal rise and fall times are equal to or less than 20 ns.

(2) Input signals are measured by 0.30 x VDDI for low state and 0.70 x VDDI for high state.

(3) Data lines can be set to "High" or "Low" during blanking time – Don't care.

Horizontal Timings for RGB I/F

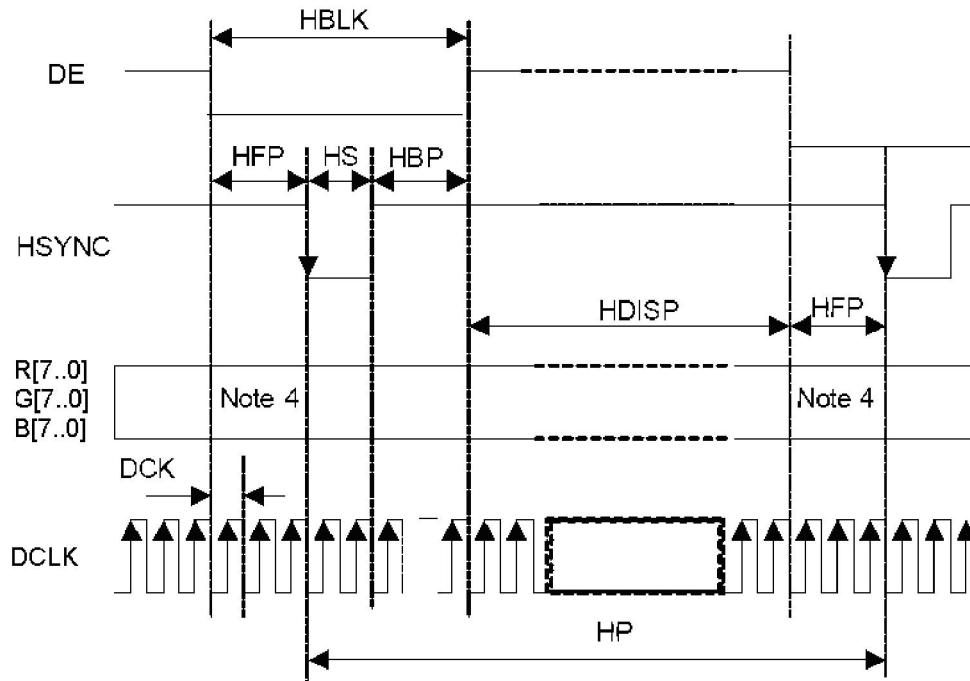


Figure 6.2-2 Horizontal Timing for RGB I/F

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
HSYNC cycle	HP	Note 3	504	-	568	DCLK
HSYNC low pulse width	HS	-	5	-	78	DCLK
Horizontal back porch	HBP	-	5	-	78	DCLK
Horizontal front porch	HFP	-	5	-	78	DCLK
Horizontal data start point	-	HS+HBP	19	-	83	DCLK
			700	-	-	ns
Horizontal blanking period	HBLK	HS+HBP+HFP	24	-	88	DCLK
Horizontal active area	HDISP	-	-	480	-	DCLK
Pixel clock frequency When RGB I/F is running	DCLK	VRR = Min. 50 Hz – Max. 70 Hz	16.3	-	25.8	MHz
			38.7	-	61	ns

Note: (1) Signal rise and fall times are equal to or less than 20 ns.

(2) Input signals are measured by 0.30 x VDDI for low state and 0.70 x VDDI for high state.

(3) HP is multiples of eight DCLK.

(4) Data lines can be set to "High" or "Low" during blanking time – Don't care.

(5) B3h Command (09h): DPL=1, the data is read on the falling edge of DCLK signal.

6.3 RGB interface General Timing

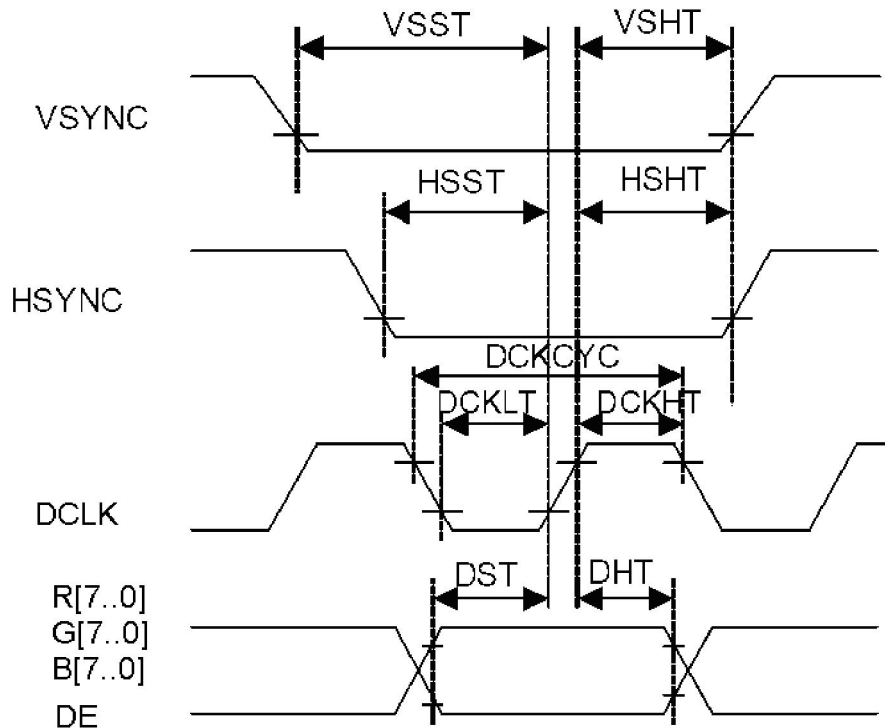


Figure 6.3-1 General Timings for RGB I/F

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Vertical sync. Setup time	VSST	-	5	-	-	ns
Vertical sync. Hold time	VSHT	-	5	-	-	ns
Horizontal sync. Setup time	HSST	-	5	-	-	ns
Horizontal sync. Hold time	HSHT	-	5	-	-	ns
Pixel clock cycle When RGB I/F is running	DCKCYC	VRR = Min. 50 Hz Max. 70 Hz	38.7 (Note1)	-	61 (Note 2)	ns
Pixel clock low time	DCKLT	-	5	-	-	ns
Pixel clock high time	DCKHT	-	5	-	-	ns
Data setup time DB[23:0]	DST	-	5	-	-	ns
Data Hold time DB[23:0]	DHT	-	5	-	-	ns

Note: (1) 25.8 MHz

(2) 16.3 MHz

6.4 Reset Input Timing

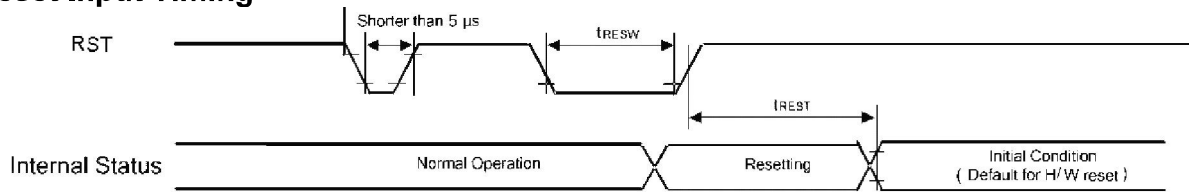


Figure 6.4-1 Write to Read and Read to Write Timing

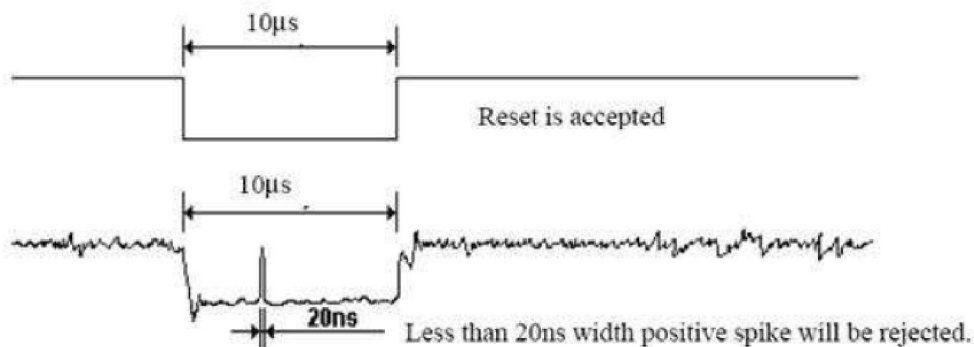
Symbol	Parameter	Related Pins	Min.	Typ.	Max.	Note	Unit
tRESW	Reset low pulse width	RST	10	-	-	-	μs
tREST	Reset complete time	-	-	-	5	When reset applied during STB mode	ms
		-	-	-	120	When reset applied during STB mode	ms

Note:

1. Spike due to an electrostatic discharge on RST line does not cause irregular system reset according to the table below.

NRESET Pulse	Action
Shorter than 5 μ	Reset Rejected
Longer than 10 μs	Reset
Between 5 μs and 10 μs	Reset Start

2. During the resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode) and then returns to Default condition for H/W reset.
3. During Reset Complete Time, ID2 value in OTP will be latched to internal register during this period. This loading is done every time when there is H/W reset complete time (tREST) within 5ms after a rising edge of RST.
4. Spike Rejection also applies during a valid reset pulse as shown below:



5. When Reset is applied during Sleep In Mode.
6. When Reset is applied during Sleep Out Mode.
7. It is necessary to wait 5msec after releasing RST before sending commands. Also Sleep Out command cannot be sent for 120msec.

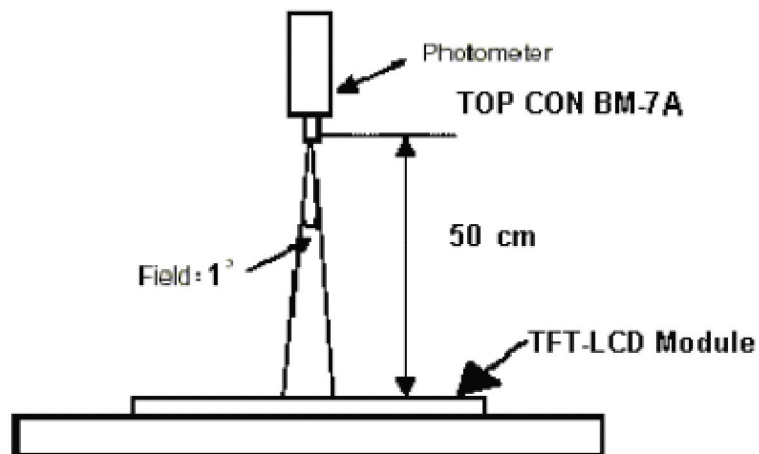
7. OPTICAL CHARACTERISTIC

Ta= 25°C

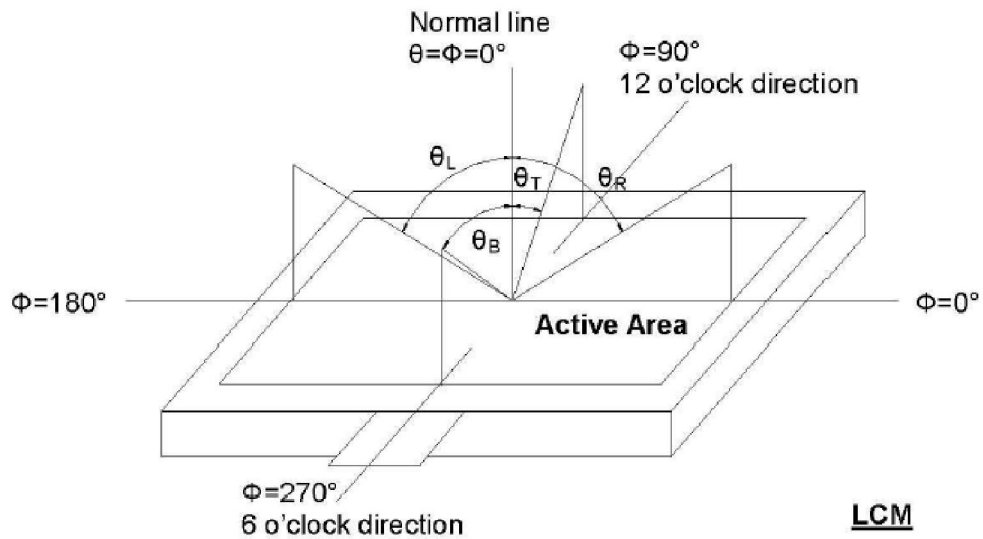
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Remarks
Viewing Angle	θL	Center CR≥10	70	80	-	deg	Note 1,2
	θR		70	80	-		
	θT		70	80	-		
	θB		70	80	-		
Contrast Ratio	CR	at optimized viewing angle	600	800	-		Note 1,4
Response time	Tr+Tf	Center θx=θy =0°	-	25	-	ms	Note 1,6
Uniformity	B-uni	θx=θy =0°	70	-	-	%	Note 1,5
Brightness	L	θx=θy =0°	800	1000	-	cd/m ²	Note 1,3
Chromaticity	W	Wx	Typ. -0.05	0.301	Typ. +0.05		Note 1,7
		Wy		0.338			

The following optical specifications shall be measured in a darkroom or equivalent state (ambient luminance ≤1 lux, and at room temperature). The operation temperature is 25°C±2°C and LED Backlight Current IF=60mA. The measurement method is shown in Note1.

Note 1: The method of optical measurement:



Note 2: Definition of viewing angle range

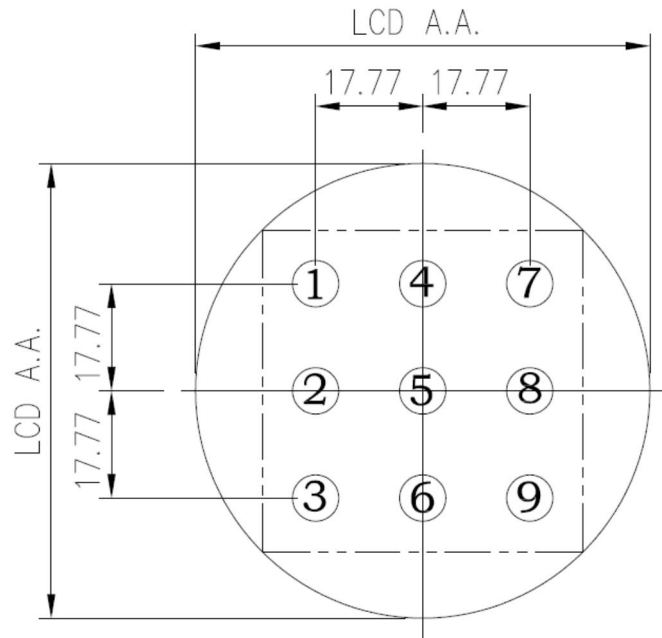


Note 3: Measured at the center area of the panel and at the viewing angle of the $\theta_x = \theta_y = 0^\circ$

Note 4: Definition of Contrast Ratio (CR):

$$CR = \frac{\text{Luminance with all pixels in white state}}{\text{Luminance with all pixels in Black state}}$$

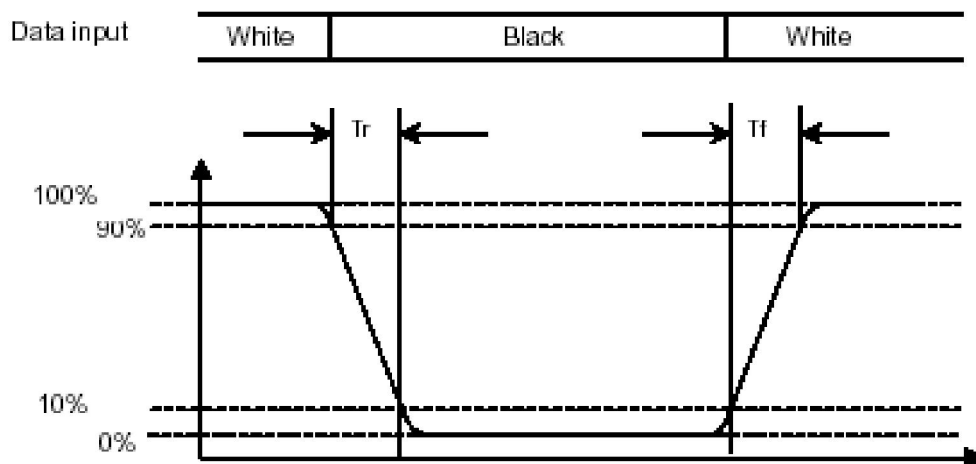
Note 5: Definition of Brightness Uniformity (B-uni):



$$B\text{-uni} = \frac{\text{Minimum luminance of 9 points}}{\text{Maximum luminance of 9 points}} \quad (\text{Note 5}).$$

Note 6: Definition of Response Time:

The Response Time is set initially by defining the "Rising Time (T_r)" and the "Falling Time (T_f)" respectively. T_r and T_f are defined as following figure.



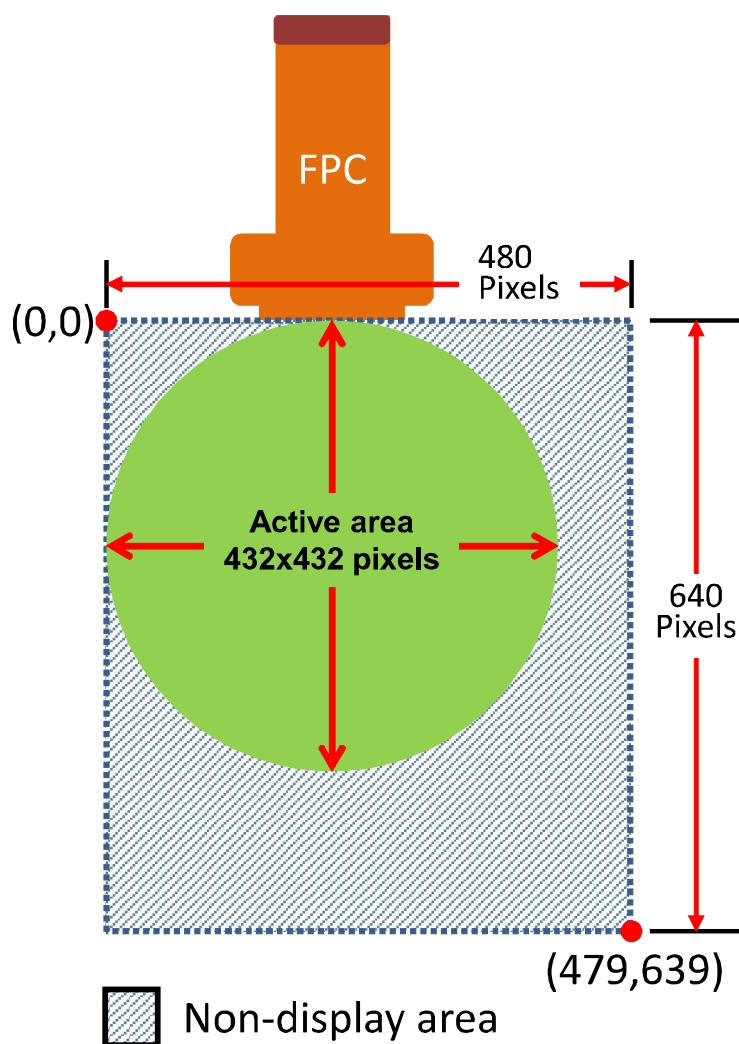
Note 7: The color coordinates (x_w, y_w) is obtained with all pixels in the viewing field at white, red, green, and blue states, respectively.

8. PIN CONNECTIONS

Pin No	Symbol	Description	Remark
1	VDDI	Power supply for interface system	
2	VDD	Power supply for analog system	
3	VDD		
4	GND	Ground	
5	/RESX	This signal will reset the device and must be applied to properly initialize the chip. Signal is active low.	
6	SDI	Serial data input signal.	
7	SDO	Serial data output signal.	
8	SCL	Serial data clock signal.	
9	CSX	Chip select input pin ("Low" enable).	
10	DCLK	Pixel clock signal.	
11	DE	Data enable signal.	
12	VSYNC	Vertical sync.	
13	HSYNC	Horizontal sync.	
14	GND	Ground	
15	DB0	RGB data bus.	
16	DB1		
17	DB2		
18	DB3		
19	DB4		
20	DB5		
21	DB6		
22	DB7		
23	GND	Ground	
24	DG0	RGB data bus.	
25	DG1		
26	DG2		
27	DG3		
28	DG4		
29	DG5		
30	DG6		
31	DG7		
32	GND	Ground	
33	DR0	RGB data bus.	
34	DR1		
35	DR2		
36	DR3		
37	DR4		
38	DR5	RGB data bus.	
39	DR6		
40	DR7		

41	GND	Ground	
42	LED+	Power Supply for LED+	
43	LED+		
44	LEDK	Power Supply for LED-	
45	LEDK		

Pixel mapping



SPI Initial Code

```
SPI_Start();
    SPI_3W_SET_CMD(0xB9);
    SPI_3W_SET_PAs(0xFF);
    SPI_3W_SET_PAs(0x83);
    SPI_3W_SET_PAs(0x63);
    SPI_Stop();
    DelayX1ms(1);

    SPI_Start();
    SPI_3W_SET_CMD(0x11);
    SPI_Stop();
    DelayX1ms(120);

    SPI_Start();
    SPI_3W_SET_CMD(0xB9);
    SPI_3W_SET_PAs(0xFF);
    SPI_3W_SET_PAs(0x83);
    SPI_3W_SET_PAs(0x63);
    SPI_Stop();
    DelayX1ms (1);

    SPI_Start();
    SPI_3W_SET_CMD(0xB1);
    SPI_3W_SET_PAs(0x78);//
    SPI_3W_SET_PAs(0x34);//
    SPI_3W_SET_PAs(0x07);//BT=7h
    SPI_3W_SET_PAs(0x33);//
    SPI_3W_SET_PAs(0x02);//
    SPI_3W_SET_PAs(0x13);//
    SPI_3W_SET_PAs(0x10);//
    SPI_3W_SET_PAs(0x10);//
    SPI_3W_SET_PAs(0x2C);//
    SPI_3W_SET_PAs(0x34);//
    SPI_3W_SET_PAs(0x22);//
    SPI_3W_SET_PAs(0x22);//
    SPI_Stop();
    DelayX1ms (1);

    SPI_Start();
    SPI_3W_SET_CMD(0x3A);
    SPI_3W_SET_PAs(0x70);
    SPI_Stop();

    SPI_Start();
    SPI_3W_SET_CMD(0xB3);
    SPI_3W_SET_PAs(0x01);
```

```
SPI_Stop();
```

```
SPI_Start();  
SPI_3W_SET_CMD(0xB4);  
SPI_3W_SET_PAs(0x00);  
SPI_3W_SET_PAs(0x12);  
SPI_3W_SET_PAs(0x72);  
SPI_3W_SET_PAs(0x12);  
SPI_3W_SET_PAs(0x06);  
SPI_3W_SET_PAs(0x03);  
SPI_3W_SET_PAs(0x54);  
SPI_3W_SET_PAs(0x03);  
SPI_3W_SET_PAs(0x4E);  
SPI_Stop();
```

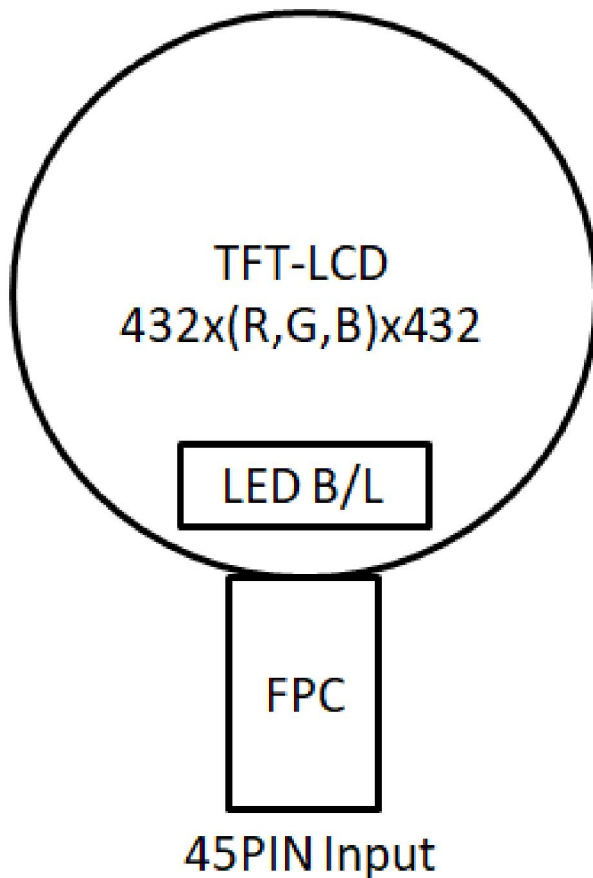
```
SPI_Start();  
SPI_3W_SET_CMD(0xB6);  
SPI_3W_SET_PAs(0x36);  
SPI_Stop();
```

```
SPI_Start();  
SPI_3W_SET_CMD(0xCC);  
SPI_3W_SET_PAs(0x07);  
SPI_Stop();  
DelayX1ms(1);
```

```
SPI_Start();  
SPI_3W_SET_CMD(0xE0); // For GP2.9" panel Gamma2.2  
SPI_3W_SET_PAs(0x00);  
SPI_3W_SET_PAs(0x00);  
SPI_3W_SET_PAs(0x00);  
SPI_3W_SET_PAs(0x1F);  
SPI_3W_SET_PAs(0x3E);  
SPI_3W_SET_PAs(0x3F);  
SPI_3W_SET_PAs(0x05);  
SPI_3W_SET_PAs(0x0B);  
SPI_3W_SET_PAs(0x0D);  
SPI_3W_SET_PAs(0xCF);  
SPI_3W_SET_PAs(0x10);  
SPI_3W_SET_PAs(0x90);  
SPI_3W_SET_PAs(0xD1);  
SPI_3W_SET_PAs(0x5C);  
SPI_3W_SET_PAs(0x1F);  
SPI_3W_SET_PAs(0x00);  
SPI_3W_SET_PAs(0x00);  
SPI_3W_SET_PAs(0x00);  
SPI_3W_SET_PAs(0x1F);  
SPI_3W_SET_PAs(0x3E);
```

```
SPI_3W_SET_PAs(0x3F);  
SPI_3W_SET_PAs(0x05);  
SPI_3W_SET_PAs(0x0B);  
SPI_3W_SET_PAs(0x0D);  
SPI_3W_SET_PAs(0xCF);  
SPI_3W_SET_PAs(0x10);  
SPI_3W_SET_PAs(0x90);  
SPI_3W_SET_PAs(0xD1);  
SPI_3W_SET_PAs(0x5C);  
SPI_3W_SET_PAs(0x1F);  
SPI_Stop();  
DelayX1ms(1);  
  
SPI_Start();  
SPI_3W_SET_CMD(0x29);  
SPI_Stop();
```

8.1 BLOCK DIAGRAM



9. QUALITY ASSURANCE

9.1 Test Condition

9.1.1 Temperature and Humidity(Ambient Temperature)

Temperature : $25 \pm 5^{\circ}\text{C}$

Humidity : $65 \pm 5\%$

9.1.2 Operation

Unless specified otherwise, test will be conducted under function state.

9.1.3 Container

Unless specified otherwise, vibration test will be conducted to the product itself without putting it in a container.

9.1.4 Test Frequency

In case of related to deterioration such as shock test. It will be conducted only once.

9.1.5 Test Method

Reliability Test Item & Level			Remark
No.	Test Item	Test Level	
1	High Temperature Storage Test	Ta=85°C,240hrs	IEC60068-2-2
2	Low Temperature Storage Test	Ta=-30°C,240hrs	IEC60068-2-1
3	High Temperature Operation Test	Ta=85°C,240hrs	IEC60068-2-2
4	Low Temperature Operation Test	Ta=-30°C,240hrs	IEC60068-2-1
5	High Temperature and High Humidity (No operation)	T=60°C,90%RH,240hrs	IEC60068-2-3
6	Thermal Cycling Test (No operation)	-30°C → +25°C → +85°C ,100 Cycles 30 min 5 min 30 min	IEC60068-2-14
7	Vibration test (Package)	Frequency:10~55HZ Amplitude:1.5mm Sweep time:11min Test period:6Cycles for each direction of X,Y,Z	IEC60068-2-6
8	Drop test (Package)	Height :60cm 1 conner,3edges,6surfaces	IEC60068-2-32
9	Electrostatic Discharge Test	Location: LCM/TP surface Condition:150pf 330Ω Contact +/- 6kV Air +/-8kV Criteria: Class C	IEC61000-4-2

9.2 Inspection condition

9.2.1 Inspection conditions

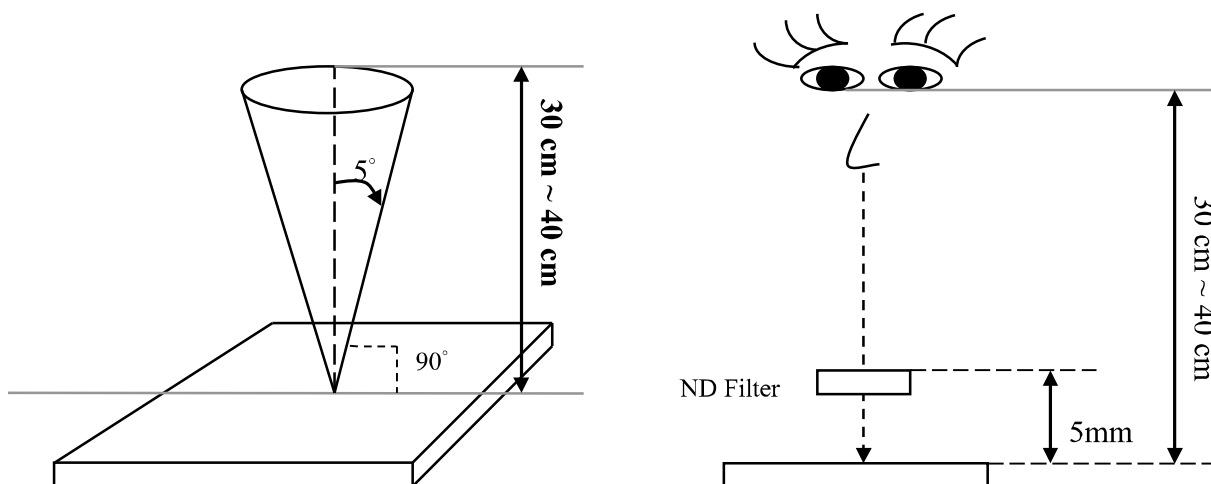
9.2.1.1 Inspection Distance : 35 ± 5 cm

9.2.1.2 View Angle :

(1) Inspection under operating condition : $\pm 5^\circ$

(2) Inspection under non-operating condition : $\pm 45^\circ$

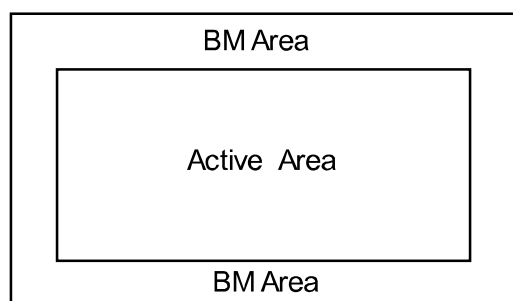
9.2.1.3 Appearance inspection time: ≤ 15 second



9.2.2 Environment conditions :

Ambient Temperature :		$25 \pm 5^\circ\text{C}$
Ambient Humidity :		$65 \pm 5\%$
Ambient Illumination	Cosmetic Inspection	600 ~ 800lux
	Functional Inspection	300 ~ 500lux

9.2.3 Definition of applicable Zones



9.3 Inspection Parameters

No.	Parameter	Criteria																		
1	Operating	Display function: No Display malfunction (Major)																		
		Line Defect: No obvious Vertical and Horizontal line defect in bright, dark and colored. (Major) (Note:1)																		
		Point Defect (Red, green, blue, dark): Active area ≤5dots (Minor)(Note:1)																		
		<table><tr><th>Item</th><th>Acceptable number</th><th>Total</th><th>Class Of Defects</th><th>AQL Level</th></tr><tr><td>Bright</td><td>2</td><td rowspan="2">5</td><td rowspan="4">Minor</td><td rowspan="4">1.5</td></tr><tr><td>Dark</td><td>3</td></tr><tr><td>Adjacent Bright</td><td>1</td><td>1</td></tr><tr><td>Adjacent Dark</td><td>1</td><td>1</td></tr></table>	Item	Acceptable number	Total	Class Of Defects	AQL Level	Bright	2	5	Minor	1.5	Dark	3	Adjacent Bright	1	1	Adjacent Dark	1	1
		Item	Acceptable number	Total	Class Of Defects	AQL Level														
		Bright	2	5	Minor	1.5														
		Dark	3																	
		Adjacent Bright	1	1																
		Adjacent Dark	1	1																
		Non-uniformity: Visible through 2%ND filter white, R, G, B and gray 50%pattern. (Minor)																		
		Foreign material in Black or White spots shape (W>1/4L) (Note: 5)																		
		<table><tr><th>Dimension</th><th>Acceptable number</th><th>Class Of Defects</th><th>AQL Level</th></tr><tr><td>D ≤ 0,3mm</td><td>*</td><td rowspan="4">Minor</td><td rowspan="4">1.5</td></tr><tr><td>0.3mm < D ≤0.5mm</td><td>4</td></tr><tr><td>Distance > 5mm</td><td></td></tr><tr><td>D> 0,5mm</td><td>0</td></tr></table>	Dimension	Acceptable number	Class Of Defects	AQL Level	D ≤ 0,3mm	*	Minor	1.5	0.3mm < D ≤0.5mm	4	Distance > 5mm		D> 0,5mm	0				
		Dimension	Acceptable number	Class Of Defects	AQL Level															
		D ≤ 0,3mm	*	Minor	1.5															
		0.3mm < D ≤0.5mm	4																	
Distance > 5mm																				
D> 0,5mm	0																			
D = (Long + Short) / 2 * : Disregard																				
Foreign Material in Line or spiral shape (W≤1/4L) (Note: 4)																				
<table><tr><th>Dimension</th><th>Acceptable number</th><th>Class Of Defects</th><th>AQL Level</th></tr><tr><td>W>0.1mm,L>7mm</td><td>0</td><td rowspan="4">Minor</td><td rowspan="4">1.5</td></tr><tr><td>L ≤ 7mm,0.05mm<W ≤0.1mm</td><td>4</td></tr><tr><td>Distance > 5mm</td><td></td></tr><tr><td>L ≤ 7mm,W<0.05mm</td><td>*</td></tr></table>	Dimension	Acceptable number	Class Of Defects	AQL Level	W>0.1mm,L>7mm	0	Minor	1.5	L ≤ 7mm,0.05mm<W ≤0.1mm	4	Distance > 5mm		L ≤ 7mm,W<0.05mm	*						
Dimension	Acceptable number	Class Of Defects	AQL Level																	
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Distance > 5mm																				
L ≤ 7mm,W<0.05mm	*																			
L : Length W : Width * : Disregard																				
2	External Inspection (non-operating)	Dimension: Outline (Major)																		
		Bezel appearance: uneven (Minor)																		
		Scratch on the Polarize: (Note:2)																		
		<table><tr><th>Dimension</th><th>Acceptable number</th><th>Class Of Defects</th><th>AQL Level</th></tr><tr><td>W>0.1mm,L>7mm</td><td>0</td><td rowspan="4">Minor</td><td rowspan="4">1.5</td></tr><tr><td>L ≤ 7mm,0.05mm<W ≤0.1mm</td><td>4</td></tr><tr><td>Distance > 5mm</td><td></td></tr><tr><td>L ≤ 7mm,W<0.05mm</td><td>*</td></tr></table>	Dimension	Acceptable number	Class Of Defects	AQL Level	W>0.1mm,L>7mm	0	Minor	1.5	L ≤ 7mm,0.05mm<W ≤0.1mm	4	Distance > 5mm		L ≤ 7mm,W<0.05mm	*				
		Dimension	Acceptable number	Class Of Defects	AQL Level															
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		L ≤ 7mm,W<0.05mm	*																	
		L : Length W : Width * : Disregard																		

		Dent and spots shape on the polarize (Note:2): (Note: 5)			
		Dimension	Acceptable number	Class Of Defects	AQL Level
		$D \leq 0.3\text{mm}$	*	Minor	1.5
		$0.3 \text{ mm} < D \leq 0.5\text{mm}$	4		
		$D > 0.5\text{mm}$	0		
		$D = (\text{Long} + \text{Short}) / 2$ * : Disregard			
		Polarizer flaw or leak out resin : Defect is defined as the active area.			

Class of defects			Definition
	Major	AQL 0.65	It is a defect that is likely to result in failure or to reduce materially the usability of the product for the intended function.
	Minor	AQL 1.5	It is a defect that will not result in functioning problem with deviation classified.

Note:1.(a)Bright point defect is defined as point defect of R,G,B with area $>1/2$ dot respectively

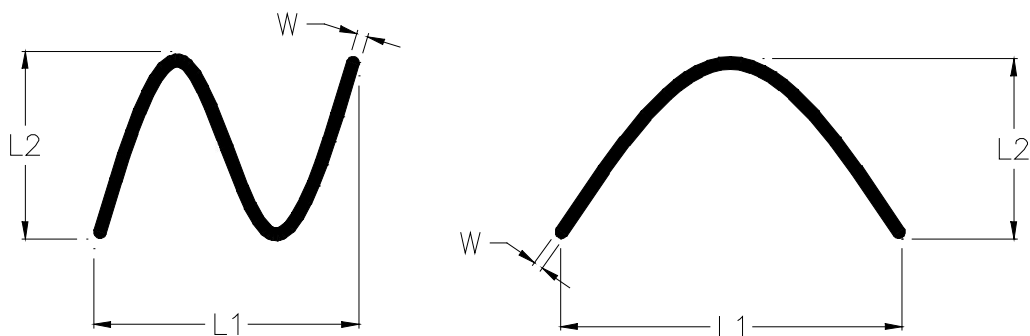
(b)Dark point defect is defined as visible in full white pattern.

(c)The point defect must under 2% ND Filter visible .

Note:2 The external inspection should be conducted at the distance $35 \pm 5\text{cm}$ between the eyes of inspector and the panel .

Note:3 Luminance measurement for contrast ratio is at the distance $50 \pm 5\text{cm}$ between the detective head and the panel with ambient illuminance less than 1 lux. Contrast ratio is obtained at optimum view angle.

Note:4 W-Width in mm , L-length of Max.(L1,L2) in mm.



9.4 Sampling Condition

Unless otherwise agree in written, the sampling inspection shall be applied to the incoming inspection of customer.

Lot size: Quantity of shipment lot per model.

Sampling type: normal inspection, single sampling

Sampling table: ISO 2859

Inspection level: Level II

10. LCM PRODUCT LABEL DEFINE

TBD

11. PRECAUTIONS IN USE LCM

1. ASSEMBLY PRECAUTIONS

- (1) You must mount a module using holes arranged in four corners or four sides.
- (2) You should consider the mounting structure so that uneven force (ex. Twisted stress) is not applied to the module. And the case on which a module is mounted should have sufficient strength so that external force is not transmitted directly to the module.
- (3) Do not touch, push or rub the exposed polarizers with glass, tweezers or anything harder than HB pencil lead. And please do not rub with dust clothes with chemical treatment.
- (4) Wipe off saliva or water drops as soon as possible. Their long time contact with polarizer causes deformations and color fading.
- (5) Do not open the case because inside circuits do not have sufficient strength.
- (6) Please do not take a LCD module to pieces and reconstruct it. Resolving and reconstructing modules may cause them not to work well.
- (7) Please do not touch metal frames with bare hands and soiled gloves. A color change of the metal frames can happen during a long preservation of soiled LCD modules.
- (8) Please pay attention to handling lead wire of backlight so that it is not tugged in connecting with inverter.

2. OPERATING PRECAUTIONS

- (1) Please be sure to turn off the power supply before connecting and disconnecting signal input cable.
- (2) Please do not change variable resistance settings in LCD module. They are adjusted to the most suitable value. If they are changed, it might happen LCD does not satisfy the characteristics specification
- (3) Be careful for condensation at sudden temperature change. Condensation makes damage to polarizer or electrical contacted parts. And after fading condensation, smear or spot will occur.
- (4) When fixed patterns are displayed for a long time, remnant image is likely to occur.
- (5) Module has high frequency circuits. Sufficient suppression to the electromagnetic interference shall be done by system manufacturers. Grounding and shielding methods may be important to minimize the interference.
- (6) Please consider that LCD backlight takes longer time to become stable of radiation characteristics in low temperature than in room temperature.

3. ELECTROSTATIC DISCHARGE CONTROL

The operator should be grounded whenever he/she comes into contact with the module. Never touch any of the conductive parts such the copper leads on the PCB and the interface terminals with any parts of the human body.

- (2) The modules should be kept in antistatic bags or other containers resistant to static for storage.
- (3) Only properly grounded soldering irons should be used.
- (4) If an electric screwdriver is used, it should be well grounded and shielded from commutator sparks.
- (5) The normal static prevention measures should be observed for work clothes and working benches; for the latter conductive (rubber) mat is recommended
- (6) Since dry air is inductive to statics, a relative humidity of 50-60% is recommended.

4. STORAGE PRECAUTIONS

- (1) When you store LCDs for a long time, it is recommended to keep the temperature between 0°C-40°C without the exposure of sunlight and to keep the humidity less than 90%RH.
- (2) Please do not leave the LCDs in the environment of high humidity and high temperature such as 60°C 90%RH
- (3) Please do not leave the LCDs in the environment of low temperature; below -20°C.

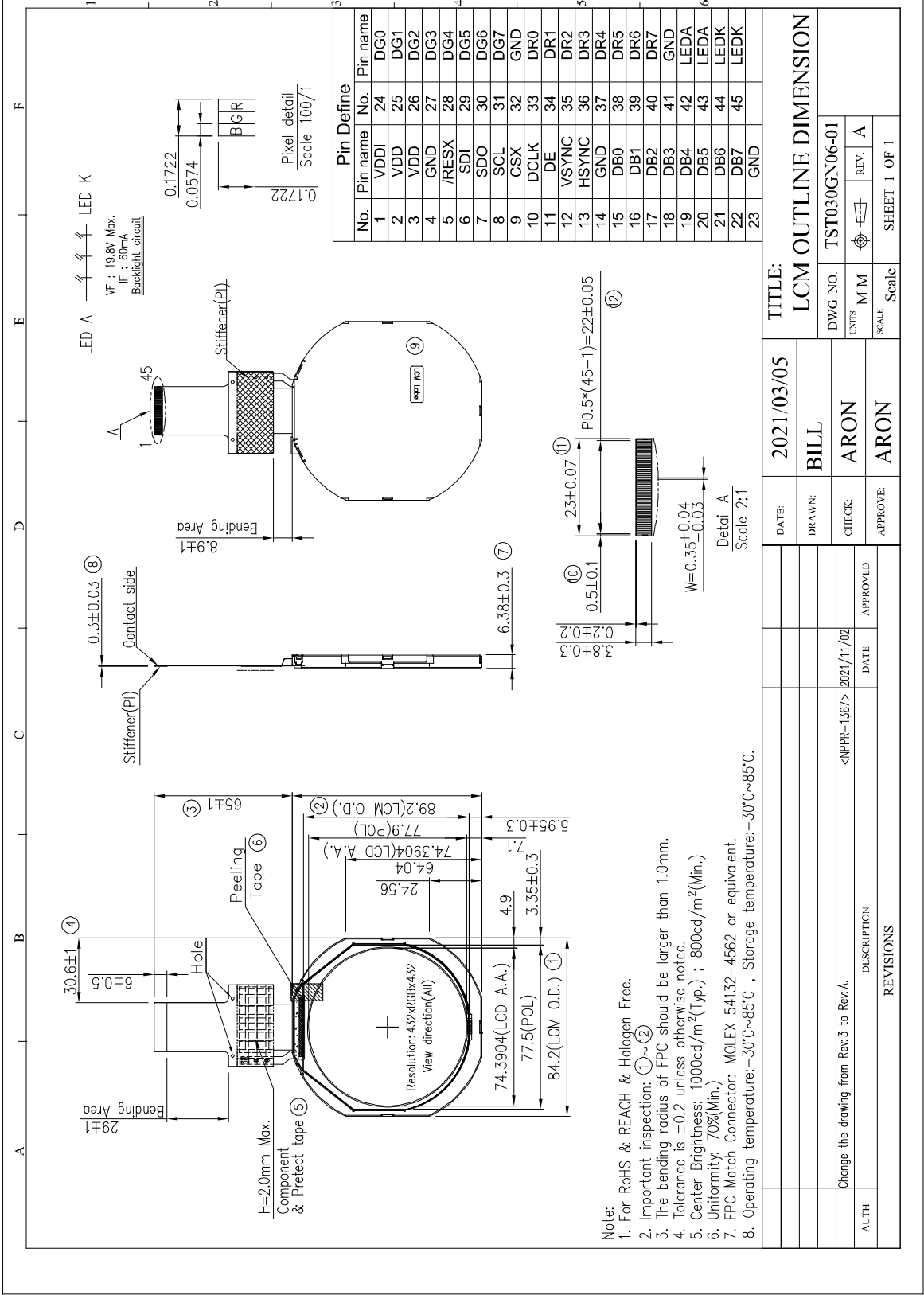
5. OTHERS

- (1) A strong incident light into LCD panel might cause display characteristics' changing inferior because of polarizer film, color filter, and other materials becoming inferior. Please do not expose LCD module direct sunlight and strong UV rays
- (2) Please pay attention to a panel side of LCD module not to contact with other materials in preserving it alone.
- (3) For the packaging box, please pay attention to the followings:
 - a. Please do not pile them up more than 5 boxes. (They are not designed so.) And please do not turn over.
 - b. Please handle packaging box with care not to give them sudden shock and vibrations. And also please do not throw them up.
 - c. Packing box and inner case for LCDs are made of cardboard. So please pay attention not to get them wet. (Such like keeping them in high humidity or wet place can occur getting them wet.)
- (4) Waste
Liquid crystal module products shall not be arbitrarily discarded; the water and soil have a negative impact on the environment, the need to be handled by a qualified unit.

6. LIMITED WARRANTY

Unless otherwise agreed between TSD and customer, TSD will replace or repair any of its LCD and LCM which is found to be defective electrically and visually when inspected in accordance with TSD acceptance standards, for a period on one year from date of shipment. Confirmation of such date shall be based on freight documents. The warranty liability of TSD is limited to repair and/or replacement on the terms set forth above. TSD will not responsible for any subsequent or consequential events.

12. OUTLINE DRAWING



13. PACKAGE INFORMATION

TBD.