GEI-100029C
(Supersedes GEI-100029B)

GE Motors & Industrial Systems

DRIVE CONTROL CARD

DS215SDCCG_A_ _

These instructions do not purport to cover all details or variations in equipment, nor to provide every possible contingency to be met during installation, operation, and maintenance. If further information is desired or if particular problems arise that are not covered sufficiently for the purchaser's purpose, the matter should be referred to GE Motors & Industrial Systems.

CONTENTS

FUNCTIONAL DESCRIPTION

WARNING

This equipment contains a potential hazard of electric shock or burn. Only adequately trained persons who are thoroughly familiar with the equipment and the instructions should install or maintain this equipment.

INTRODUCTION

This instruction book addresses only drive applications of the DS215SDCCG_A_ _ card (SDCC). The SDCC contains the primary control circuitry and software for a drive or exciter. The SDCC consists of three 16-bit microprocessors and associated circuits coupled via dual-ported RAM. (Dual-ported RAM [DPR] is RAM configured as memory arrays that can be independently and simultaneously accessed by two microprocessors.)

The SDCC also includes interface circuitry that connects with other boards to form various types of ac and dc motor drives. The interface circuitry controls and processes drive and motor signals, and customer I/O. (The interface circuitry and three main microprocessors are used for other functions in TC2000 applications.) The SDCC's three main microprocessors are:

- Drive Control Processor (DCP). An 80C186 microcontroller (U1) with numerous built-in peripheral functions and uses both digital and analog I/O.

These functions include address decoding for chip selects, wait-state generators, an interrupt controller, timer/counters, and the direct memory access (DMA) controller. DCP software consists of user interfaces, outer regulating loops (such as speed and position), and system level functions.

- Motor Control Processor (MCP). An 80C196 microcontroller (U21) with high-speed I/O, conventional digital I/O, analog I/O, timer/counters, and a watchdog timer. MCP software consists of inner loops such as current regulators, and motor/technology specific functions such as dc phase control, ac motion control, and ac general purpose.
- Co-motor Processor (CMP). A TMS320C25 digital signal processor (U35) that performs math-intensive functions for motor control algorithms too complex for the MCP. The SDCC uses this processor and its associated circuitry only when the drive requires the additional processing capability. The CMP interfaces only to its EPROM and MCP/CMP dual-ported RAM.

The DS215SDCC card includes onboard software stored in five memory chips: four EPROMs (U11, U12, U22, and U23) that contain configuration data programmed at the factory and one EEPROM (U9) that contains field-adjustable parameters. These memory chips are contained in sockets on the SDCC.

When ordering replacement boards, note that the DS200SDCC card does not include the five memory chips mentioned above (the sockets are empty).

NOTE

When replacing a DCC, specify a DS215SDCC card as a replacement to ensure that the five memory chips are included.

CARD GROUPS

There are currently three group numbers of the SDCC available (G2 versions were never manufactured). The variations between the groups are as follows:

- DS200SDCCG1A_ _: Used in AC2000, DC2000, and EX2000 drive applications
- DS200SDCCG3A_ _: Variation of SDCC that has reduced functionality (used in DC1000 drives)
- DS200SDCCG4A_ _: Used in TC2000 turbine applications (same as G1A except with enlarged EE parameter storage area and different firmware)

CARD CONNECTIONS

The SDCC interfaces with the other boards of the controller and external signals via eight connectors (designated _PL). See Figure 3 for an SDCC layout diagram showing the locations of the connectors and Tables 3 – 9 for the pin signals of each connector. Connectors to other boards are as follows:

- 1PL – I/O between the Power Supply/Interface Board (DS200IMCP, DCI, SDCI, or DCFB) and the SDCC
- 2PL – ±5, 15, and 24 V dc inputs from the Power Supply/Interface Board to the SDCC
- 3PL – SDCC outputs to the LAN Communications Card (DS215SLCC)
- 6PL – I/O between the Drive Terminal Board (531X305NTB) or Simple Drive Terminal Board (DS200STBA) and the SDCC
- 7PL – I/O between the Signal Processor Card (531X309SPC) or Multibridge Signal Processing Card (DS200SPCB) and the SDCC (not present on SDCCG3s)
- 8PL – I/O between the Drive Terminal Board (531X305NTB) or Simple Drive Terminal Board (DS200STBA) and the SDCC
- 9PL – Not Used (not present on SDCCG3s)
- 11PL – SDCC outputs to meters (not present on SDCCG3s)

AUXILIARY BOARD MOUNTING PROVISIONS

The SDCC has mounting provisions for other auxiliary boards and modules. The following boards can be mounted on the SDCC:

- DS215SLCC or 531X306LCC LAN Communications Card
- 531X309SPC Signal Processor Card
- DS200SPCB Multibridge Signal Processor Card

LED DISPLAY

A bank of 10 diagnostic LEDs is provided on the SDCC and displays fault codes in either **BCD** (binary coded decimal) or **binary** form, depending on the fault number (see Figure 3 for location). The LEDs indicate faults in a blinking mode as follows:

- Faults 1 to 399
  - slow blink rate
  - BCD pattern (left-most two LEDs encode the hundreds digit; next four, the tens digit; right-most, the units digit; see Figure 1)

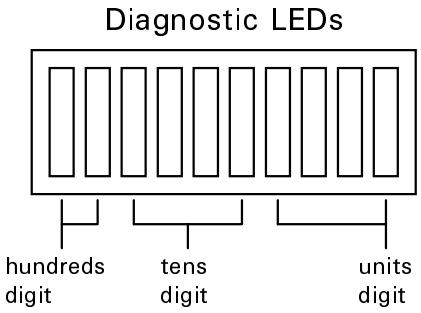

Figure 1. BCD-coded LED Display

- Faults 400 to 1023
  - faster blink rate
  - binary pattern (left-most LED is 2^9 [or 512], second-most LED is 2^8 [or 256], and so on; see Figure 2)
- No fault or drive not running
  - sequential blinking, two at a time
  - blinking from outer positions inward to center, and back

These same LEDs can be set by software jumper to also coarsely display drive variables when running. (For example, displayed in an absolute or signed bar graph mode). Setting software jumpers this way does not inhibit the LED fault display.

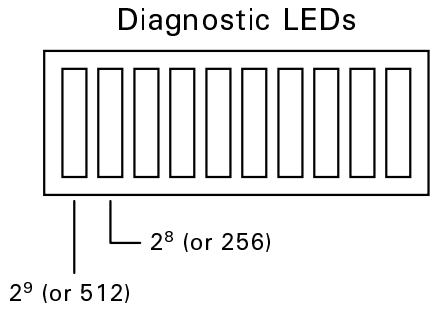

Figure 2. Binary-coded LED Display

RESET CIRCUITS

The SDCC provides four reset circuits, including a RESET pushbutton.

CAUTION

The system trips when a hard reset is initiated; the system should not normally be reset when running.

A reset can be generated in four ways:

- By pressing the RESET pushbutton on the SDCC (See Figure 3 for location.)
- By applying +5 to +24 V dc to customer interface points on the STBA or NTB/3TB boards (These points interface with the SDCC through 6PL.)
- By the SDCC generating a reset via programmed software control
- By the SDCC generating a reset via automatic internal hardware watchdog protection.

APPLICATION DATA

TESTPOINTS

The SDCC includes onboard testpoints for test and troubleshooting purposes. Testpoints are metal posts located in specific signal paths. These signals can be measured or viewed on an oscilloscope or other measuring instrument. Table 1 lists and defines each testpoint. Figure 3 shows testpoint locations.

CONFIGURABLE HARDWARE

The SDCC includes configurable hardware that must be set correctly for the application:

- Berg-type (manually movable) hardware jumpers, identified by a *JP* nomenclature (see Table 2)
- Wire jumpers, identified by a *WJ* nomenclature (see Table 2)

These jumpers are used for factory test or user application options. Most of the jumper selections have been factory set. The test data sheets supplied with each controller (in the drive/exciter door pocket) indicate these factory set positions. Table 2 lists the jumper descriptions, showing the default setting first.

Figure 3 is a layout diagram of the SDCC, showing the locations of all jumpers.

SOFTWARE CONFIGURATION TOOLS

Any adjustment, downloading, or replacement of software on the SDCC requires the use of the ST2000, GE Control System Toolbox, or LynxOS™ Drive Configurator. The applicable drive/exciter instruction book, an appropriate PC, and the ST2000, GE Control System Toolbox, or LynxOS Drive Configurator instruction book are also required for any software adjustments.

- ST2000 is a DOS based set of software tools for configuring GE DIRECTO-MATIC® 2000 control equipment. Refer to GEH-5860 for complete information on these tools.
- The GE Control System Toolbox is a Windows™ based set of software tools for configuring GE DIRECTO-MATIC® 2000 control equipment. Refer to GEH-6333 for complete information on the toolbox.
- The LynxOS Drive Configurator is a set of software tools for configuring GE DIRECTO-MATIC 2000 control equipment. It is designed to run on a personal computer (PC) operating with the LynxOS operating system. Refer to GEH-6203 for complete information on these tools.

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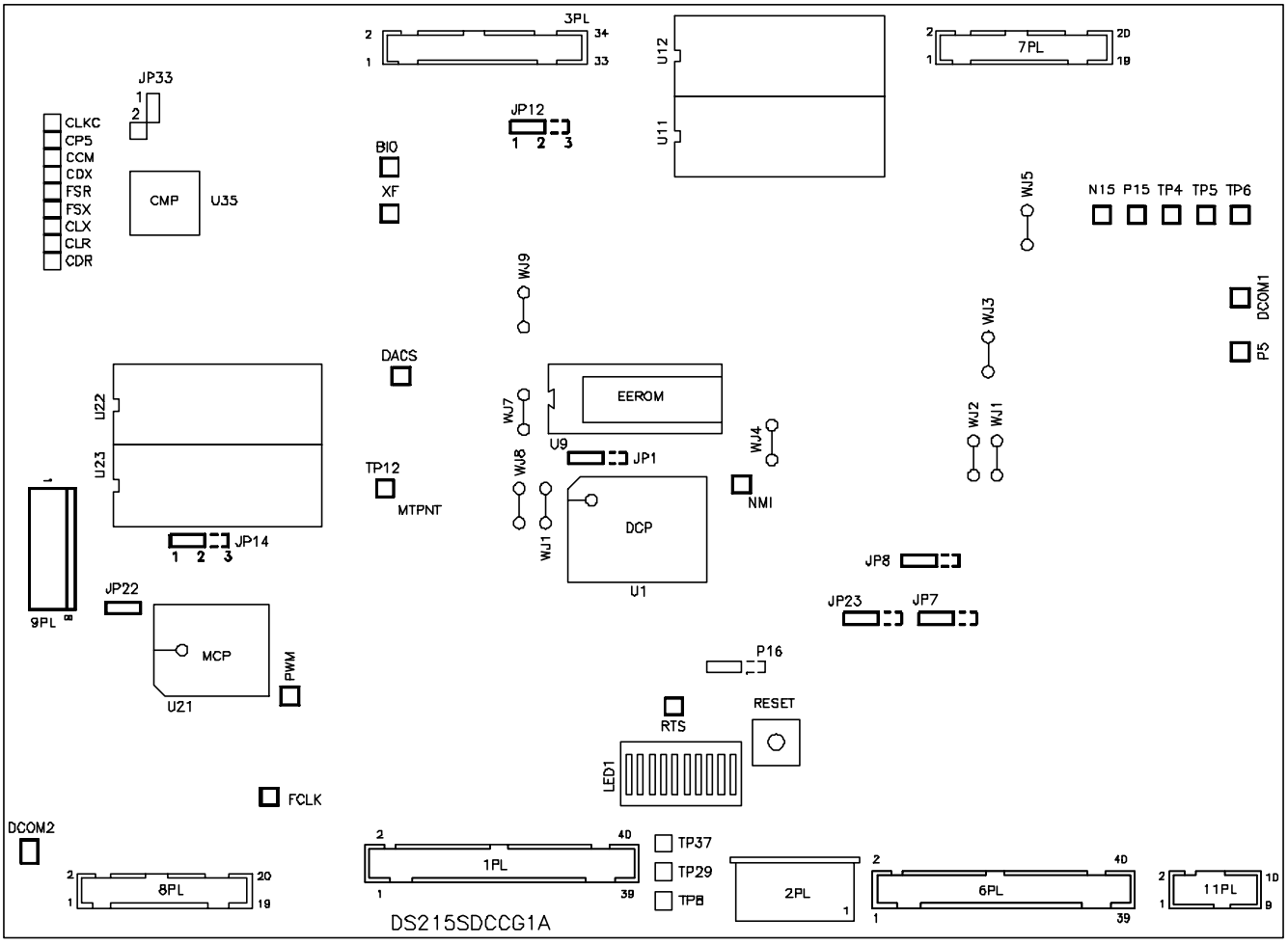

Figure 1. SDCC Layout Diagram

I/O TABLES

Tables 3 – 9 list the I/O pin signals of the different connectors on the SDCC. The tables are organized as follows:

- **Table 3** – 1PL, I/O between the IMCP, DCI, SDCI, or DCFB board and SDCC
- **Table 4** – 2PL, Power inputs from the IMCP board to the SDCC
- **Table 5** – 3PL, SDCC outputs to the SLCC
- **Table 6** – 6PL, I/O between NTB/3TB or STBA board and the SDCC
- **Table 7** – 7PL, I/O between the SPC or SPCB board and the SDCC (not present on SDCCG3s)
- **Table 8** – 8PL, I/O between the NTB/3TB or STBA board and the SDCC
- **Table 9** – 11PL, SDCC outputs to meters (not present on SDCCG3s)

Table 1. SDCC Testpoints

Name	Description
DCOM1	0 volt common reference point for test signals, same as DCOM2
DCOM2	0 volt common reference point for test signals, same as DCOM1
P5	Testpoint for regulated +5 volt (±5%) power supply
TP4	DCP foreground timing flag (720 Hz)
TP5	DCP blockware timing flag (720 Hz)
TP6	DCP slow background timing flag (90 Hz)
RTS	Unused. General purpose testpoint output from DCP
TP8	Analog representation of phase A motor current, with a nominal dc offset of +2.5 V
FCLK	“I'm alive” 8 MHz oscillator output from MCP
NMI	Initiates board test (Test 13) when momentarily tied to +5 volts. For board test only, not recommended for use in a drive environment.
DACS	Diagnostic D/A converter daughter board select (used with auxiliary diagnostic hardware in conjunction with EE.600)
N15	Testpoint for regulated -15 volt (±5%) power supply
P15	Testpoint for regulated +15 volt (±5%) power supply
CDR*	TMS320 serial data receive
CDX*	TMS320 serial data transmit
CLX*	TMS320 serial transmit clock input
CLR*	TMS320 serial receive clock input.
FSX*	TMS320 serial frame sync pulse for transmit
FSR*	TMS320 serial frame sync pulse for receive
CLKC*	TMS320 clock oscillator input
CP5*	+5 V power supply to TMS320 diagnostic D-A daughter board
CCM*	Common power supply return for TMS320 diagnostic D-A daughter board
TP29	Testpoint for input line frequency
TP37	Testpoint for dc voltage; Not used on ac drives

**The row of testpoints in the upper left corner of the SDCC (CDR, CDX, CLX, CLR, FSX, FSR, CLKC, CP5, and CCM) is reserved for diagnostic purposes for the TMS320C25 processor, via a daughter board which allows serial diagnostic D-A converters to be added for development/test purposes only.*

Table 2. SDCC Jumpers and Wire Jumpers

Revision	Name	Description
All	JP1	EEPROM parameter write protect 1.2 Write inhibited, safe mode 2.3 Write enabled, must be in this position to modify EEPROM
All	JP7	Enable 6:1 gain increase for feedback voltage controlled oscillator (VCO) circuitry 1.2 Normal gain 2.3 Increased gain
All	JP8	Enable absolute value circuit for feedback VCO circuitry Note that, due to the 10 V maximum voltage available on the Simple Drive Terminal Board (STBA), the feedback VCO is not normally suitable for analog tachs unless the Drive Terminal Board (NTB/3TB) is used. 1.2 Bipolar mode for dc tachometers 2.3 Absolute mode for analog ac
0–ACZ	JP15	Enable for DCP crystal 1.2 Enabled (required for normal operation) 0 Manufacturing test only
All	JP16	Enables FLASH electrically erasable program memory erase/reprogram mode 1.2 Normal mode for EPROM or Flash memory read only 2.3 Reserved for Flash memory reprogramming mode
All	JP22	Enable for MCP crystal 1.2 Enabled (required for normal operation) 0 Manufacturing test only
All	JP23	Signal source into DCP's external DMA channel (used for time tagged inputs) 1.2 From NTB/3TB analog feedback input (for ac AN tach interfaces) 2.3 From NTB/3TB encoder marker track input (EOM)
0–ACZ	JP33	Enable for CMP crystal 1.2 Enabled (required for normal operation) 0 Manufacturing test only
ADB–Pres	WJ1	Remap MET3 D/A to DAC1 output for SDCCG3 SDCCG3 omits the 12-bit D/A converter used for DAC1 and DAC2, and instead drives these outputs with the 8-bit D/A used to drive MET3 and MET4 on SDCCG1. MET3 and MET4 are not available on the SDCCG3. If this jumper is erroneously present on an SDCCG1 card, the D/A outputs will be corrupted; if the jumpers are missing on an SDCCG3 card, the DAC1/ DAC2 output will not function. 0 SDCCG1, jumper omitted 1.2 SDCCG3, jumper installed
ADB–Pres	WJ2	Remap MET4 D/A to DAC2 output for SDCCG3 0 SDCCG1, jumper omitted 1.2 SDCCG3, jumper installed
ADB–Pres	WJ3	Provide 10-volt full scale reference for D/A outputs on SDCCG3 If this jumper is set incorrectly for the SDCC group number, the D/A converters will operate improperly. 0 SDCCG1, uses internal reference from 12-bit D/A, jumper omitted 1.2 SDCCG3, develops reference from +5 V dc power supply
ADB–Pres	WJ4	Identify card group to firmware The firmware uses this jumper to identify whether the card contains G1 or G3 components. Incorrect setting of this jumper will cause malfunction of the DCP, including inability of processor to powerup and configure card logic cell arrays, and possible loss of EEPROM drive configuration memory. 0 Omit jumper. Identifies card as group G1 1.2 Install jumper. Identifies card as group G3
ADB–Pres	WJ5	Configure card for logic cell array (LCA) size Incorrect setting of this jumper may damage or cause unreliable operation of LCA U32. 0 Jumper omitted on SDCC G3 (LCA is 3042 device) 1.2 Jumper installed on SDCC G1 (LCA is 3064 device)

Table 2. SDCC Jumpers and Wire Jumpers — Continued

Revision	Name	Description
ADB–Pres	WJ7	Configure card for EEPROM size In all present drive applications, WJ7 and WJ9 must be omitted and WJ8 and WJ10 must be installed. The alternate setting allows for future expansion of EEPROM size from 32K to 64K bytes. Incorrect setting of these jumpers will result in incorrect reading and configuration of the drive EEPROM. 0 SDCC G1 and G3, jumper omitted 1.2 Reserved for future expansion
ADB–Pres	WJ8	Configure card for EEPROM size 0 Reserved for future expansion, jumper omitted 1.2 Jumper installed on SDCCG1 and SDCCG3
ADB–Pres	WJ9	Configure card for EEPROM size 0 Jumper omitted on SDCCG1 and SDCCG3 1.2 Reserved for future expansion
ADB–Pres	WJ10	Configure card for EEPROM size 0 Reserved for future expansion, jumper omitted 1.2 Jumper installed on SDCCG1 and SDCCG3

Table 3. Connector 1PL (AC2000 Drives Only), I/O Between SDCC and Power Supply Board

Pin No.	Nomenclature	Description
1	DPSEN	Driver power state
2	DBDUTY	DB IGBT ON signal
3	PHLOSS	Ac line phase loss signal
4	VTHRM	Variable voltage output of IIBD temperature sensor circuit
5	VMAG	Ac line-to-line peak for magnitude detection
6	VSEQ	Ac line voltage for phase sequence detection
7	----	Not connected
8	/IA	Buffered phase A VCO current feedback from IIBD board
9	/IB	Buffered phase B VCO current feedback from IIBD board
10	/IC	Buffered phase C VCO current feedback from IIBD board
11	V(B-A)	Phase (B-A) VCO voltage feedback
12	V(C-A)	Phase (C-A) VCO voltage feedback
13	VDC	Dc link voltage feedback VCO output
14	SYOSC	Burst oscillator
15	----	Not connected
16	U/DA	Up/down command phase A
17	U/DB	Up/down command phase B
18	U/DC	Up/down command phase C
19	DBTST	DB turn-on signal

Table 3. Connector 1PL (AC2000 Drives Only) — Continued, I/O Between SDCC and Power Supply Board

Pin No.	Nomenclature	Description
20	ENA	Enable phase A IGBT gate drive circuit
21	ENB	Enable phase B IGBT gate drive circuit
22	ENC	Enable phase C IGBT gate drive circuit
23	ENDB	Enable DB IGBT
24	SS1	Soft-start SCR gate enable
25	SS2	Same as SS1 (pin 24)
26	SS3	Same as SS1 (pine 24)
27	/FLTRST	Fault reset
28	FAULT2	Inverter gate drive fault signal
29	LINESYNC	Ac line synchronizing signal
30	FAULT1	DB overvoltage trip signal
31	/RST1	System reset
32, 33	------	Not connected
34	MAC	MA contactor control from SDCC card
35 - 37	----	Not connected
38	DTYPE	Drive type identifier (3.3 - 3.8 V dc for an AC2000 IGBT drive)
39, 40	------	Not connected

Table 4. Connector 2PL (AC2000 Drives Only), Power Inputs From Power Supply Board

Pin No.	Nomenclature	Description
1	/PSEN	Power supply enable
2	N15	Negative 15 V dc to the SDCC, SLCC, and NTB/3TB or STBA boards
3	P15	Positive 15 V dc to the SDCC, SLCC, and NTB/3TB or STBA boards
4	DCOM	±15 V dc common to the SDCC, SLCC, and NTB/3TB or STBA boards
5	P5	Positive 5 V dc to the SDCC, SLCC, and NTB/3TB or STBA boards
6	P5	Positive 5 V dc to the SDCC, SLCC, and NTB/3TB or STBA boards
7	DCOM	Positive 5 V dc common to the SDCC, SLCC, and NTB/3TB or STBA boards
8	N24	Negative 24 V dc to the SDCC, SLCC, and NTB/3TB or STBA boards
9	P24	Positive 24 V dc to the SDCC, SLCC, and NTB/3TB or STBA boards

Table 5. Connector 3PL,
SDCC Output To SLCC

Pin No.	Nomenclature	Description
1 - 8	BD0 - BD7	Buffered, demultiplexed SDCC Drive Control Processor (DCP) data bus lines 0 - 7
9	DCOM	Power supply return (common)
10	P5	Positive 5 V dc regulated power supply for digital circuitry
11	/RST3	System reset signal (active low)
12	LINT	Interrupt from SLCC/SDCC microapplication chip to DCP
13	/LBSY	Busy bus control handshake to DCP
14	BA12	Buffered address latch enable from DCP
15	DCOM	Power supply return (common)
16	/BCSL	SLCC chip select
17	/BRD	Buffered read control line from DCP
18	/BWR	Buffered write control line from DCP
19	BA8	Buffered, demultiplexed DCP address line 8
20	BA9	Buffered, demultiplexed DCP address line 9
21	/BCSU	SDCC microapplication chip select
22	BA10	Buffered, demultiplexed DCP address line 10
23	BA11	Buffered, demultiplexed DCP address line 11
24	DCOM	Power supply return (common)
25	DCOM	Power supply return (common)
26	P5	Positive 5 V dc regulated power supply for digital circuitry
27 - 34	BA0 - BA7	Buffered, demultiplexed DCP address lines 0 through 7

Table 6. Connector 6PL,
I/O Between SDCC and NTB/3TB or STBA Boards

Pin No.	NTB/3TB Terminal	STBA Terminal	Nomenclature	Description
1	42	------	CTLN1	CTLN1 and CTLN2 form part of the circuit for picking up the MA contactor pilot relay and must be connected together to allow the drive to run. They provide both a place to connect external interlocks and provide a fail-safe (microprocessor independent) means of stopping the drive.
2	44	------	CTLN2	See CTLN1
3	--	------	LBIAS	±24 V dc bias for digital inputs from NTB/3TB (for +/- logic)
4	61	------	T0OUT	TTL output through 200 W from timer/counter 0 of SDCC's Drive Control Processor.
5	34	------	RUN	General-purpose digital input defaulted to, but not limited to, RUN function
6	36	------	JOG	General-purpose digital input defaulted to JOG function
7	38	------	POL	General-purpose digital input defaulted to the reference polarity function
8	40	------	XSTP	General-purpose digital input defaulted to the XSTOP function (normally closed)
9	47	------	MSRF	Relay #6 coil driver (Master Sync Reference output), open collector driver output
10 - 14	------	------	RO1 - RO5	NTB/3TB relay coil output driver lines 1 through 5
15	------	------	P3B	Scalable general-purpose analog input from NTB/3TB
16	------	------	P4B	Scalable general-purpose analog input from NTB/3TB
17	51	------	ASP0	Medium resolution analog input with fixed scaling for ±5 V dc maximum from NTB/3TB
18	------	------	VC3NB	Inverting differential analog input for SDCC auxiliary VCO #3
19	------	------	VC3PB	Non-inverting differential analog input for auxiliary VCO #3
20, 21	------	------	P1B, P2B	Scalable general-purpose analog inputs from NTB/3TB
22	------	------	------	Not connected
23	49	------	DVM	Medium resolution analog input channel with fixed scaling for ± 51.0 V dc maximum
24	53	34	DA1	Output from 8-bit (DCC and SDCCG3) or 12-bit (SDCCG1) D/A converter. Can source ±10 V dc at no load or ±8 V dc at a 10 mA load (200 W series impedance). Any drive variable can be sent to this output and can be scaled to set the value corresponding to 10 V dc output. (For diagnostics and system applications)
25	55	35	DA2	See DA1 (pin 24)

Table 6. Connector 6PL — Continued,
I/O Between SDCC and NTB/3TB or STBA Boards

Pin No.	NTB/3TB Terminal	STBA Terminal	Nomenclature	Description
26	54	36	MET1	Output from 8-bit D/A converter. Can source ±10 V dc at no load or ±8 V dc at a 10 mA load (200 W series impedance). Any drive variable can be sent to this output and can be scaled to set what value corresponds to 10 V dc output. (Provided for meter driver functions)
27	56	37	MET2	See MET1 (pin 26)
28	57	------	MSSY	Input to internal interrupt (INT0) of DCP Is biased to +24 V dc through 27 kW and must be pulled to COM (less than +1.5 V dc) to be recognized by DCP.
29	59	------	T0IN	Input to internal timer/counter 0 of Drive Control Processor (DCP, located on SDCC) Is biased to +24 V dc through 27 kW and must be pulled to COM (less than +1.5 V dc) to be recognized by DCP.
30	58	38	RESET	Hard reset input to the drive Connecting RESET to +5 to +24 V dc causes all processors in the drive to be reset. Leaving RESET open or connecting to COM allows drive operation. The SDCC provides a 20 ms noise filter on this input.
31	------	------	TDB	RS-232C channel transmitted from DCP
32	------	------	RDB	RS-232C channel received by DCP
33	------	------	CTSB	RS-232C channel clear-to-send handshake
34	------	------	RTSB	RS-232C channel clear-to-receive handshake
35	------	------	VC4NB	Inverting differential analog input for SDCC auxiliary VCO #4
36	------	------	VC4PB	Non-inverting differential analog input for auxiliary VCO #4
37	------	43	RFNB	Differential analog input from NTB/3TB to reference VCO, negative line
38	------	41	RFPB	Same as pin 37, but positive line
39	------	49	FBNB	Differential analog input from NTB/3TB to feedback VCO, negative line
40	------	46	FBPB	Same as pin 39, but positive line 3

Table 7. Connector 7PL,
I/O Between SDCC and SPC or SPCB Board

Pin No.	Nomenclature	Description
1	SPA1	±5 V dc SPC/SPCB analog channel #1
2	SPA2	±5 V dc SPC/SPCB analog channel #2
3	E1Z	Marker channel from encoder #1 interface
4	E2Z	Marker channel from encoder #2 interface
5	N15	Negative 15 V dc power supply for analog circuitry on SPC/SPCB
6	P15	Positive 15 V dc power supply for analog circuitry on SPC/SPCB
7	DCOM	Power supply return (common)
8	SPRS	Digital output from DCP to SPC/SPCB
9	DCOM	Power supply return (common)
10	P5	Positive 5 V dc power supply for digital circuitry on SPC/SPCB
11	E1UP	Up channel output from encoder #1 interface
12	E1DN	Down channel output from encoder #1 interface
13	E2UP	Up channel output from encoder #2 interface
14	E2DN	Down channel output from encoder #2 interface
15	0RST7	System reset (active low). Not connected on SPCB card
16	DCOM	Power supply return (common)
17	SPSYN	Not connected on SPC card. Sync pulse listener input to SDCC for SPCB card
18	SPSYO	Not connected on SPC card. Sync pulse output from SDCC for SPCB card
19	SPTX	5 V dc output from SDCC's Motor Control Processor (MCP) UART
20	SPRX	5 V dc input to MCP UART

Table 8. Connector 8PL,
I/O Between SDCC and NTB/3TB or STBA Boards

Pin No.	NTB/3TB Terminal	STBA Terminal	Nomenclature	Description
1	6	------	FA	Non-inverting RS-422 half-duplex serial data line from the SDCC's Motor Control Processor (MCP) UART
2	8	------	FB	Inverting RS-422 half-duplex serial data line from MCP UART
3	10	7	DCOM	Signal return for EXSY (at COM potential)
4	12	------	EXSY	External sync input to MCP
5	------	------	------	Not connected
6	1	1	E0AB	Encoder interface Channel A non-inverted differential input
7	3	3	/E0AB	Encoder interface Channel A inverted differential input. (Tie to COM for single-ended encoders)
8	5	5	E0BB	Encoder interface Channel B non-inverted differential input
9	7	6	/E0BB	Encoder interface Channel B inverted differential input. (Tie to COM for single-ended encoders)
10	9	------	E0MB	Encoder interface marker pulse channel non-inverted differential input
11	11	------	/E0MB	Encoder interface marker pulse channel inverted differential input. (Tie to COM for single-ended encoders)
12	------	------	------	Not connected
13	14	9	CI1	CI1 – CI8 are general-purpose control inputs, ±24 V dc maximum with 27 kW input impedance
14	16	11	CI2	See CI1 (pin 13)
15	18	13	CI3	See CI1 (pin 13)
16	20	15	CI4	See CI1 (pin 13)
17	22	17	CI5	See CI1 (pin 13)
18	24	19	CI6	See CI1 (pin 13)
19	26	21	CI7	See CI1 (pin 13)
20	28	50	CI8	See CI1 (pin 13)

Table 9. Connector 11PL,
SDCC Output to Meters

Pin No.	Nomenclature	Description
1, 2	------	Not connected
3	DCOM	Drive common connection
4	MTR1	MTR1 through MTR4 are outputs from an 8-bit D/A converter and can source ±10 V dc at no load or ±8 V dc at 10 mA load (200 W series impedance). Any drive variable can be steered to these D/A outputs and can be scaled to set what value corresponds to the 10 V dc output. These outputs are for meter driver functions.
5	MTR2	See MTR1
6	MTR3	See MTR1
7	MTR4	See MTR1
8	DCOM	Drive common connection
9, 10	------	Not connected

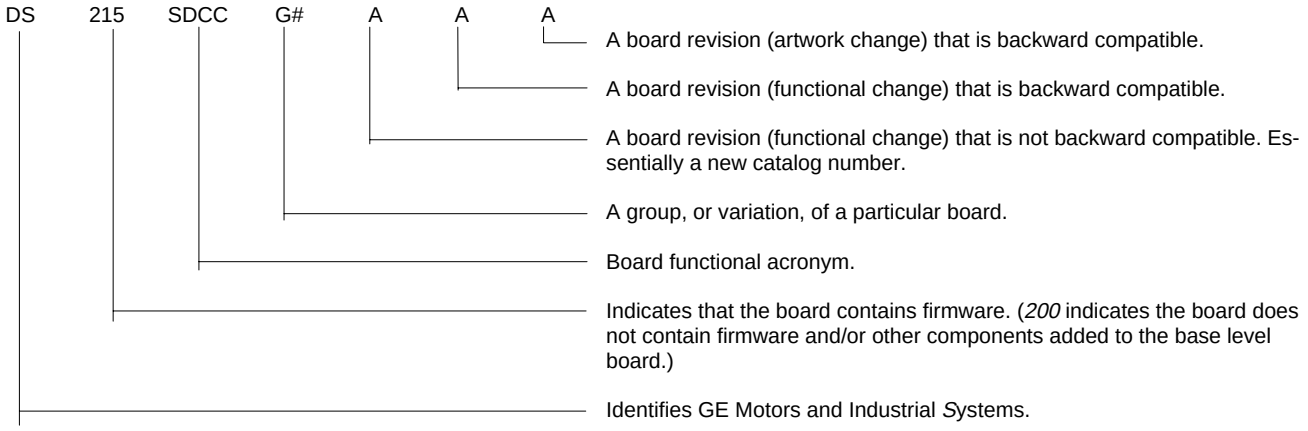

Figure 4. Sample Board Part Number, DS Series

RENEWAL/WARRANTY REPLACEMENT

BOARD IDENTIFICATION

A printed wiring board is identified by an alphanumeric part (catalog) number stamped on its edge. For example, the Drive Control Card, with onboard software, is identified by part number DS215SDCCG#ruu. (See Figure 4 for part number breakdown.)

NOTE

All digits are important when ordering or replacing any board.

The DS215SDCC card includes onboard software stored in five memory chips: four EPROMs (U11, U12, U22, and U23) that contain configuration data programmed at the factory, and one EEPROM (U9) that contains field-adjustable parameters. These memory chips are contained in sockets on the SDCC.

When ordering replacement boards, note that the DS200SDCC card does not include the five memory chips mentioned above (the sockets are empty).

NOTE

The SDCC may also be used to replace a 531X301DCC Drive Control Card (DCC). These instructions include information for replacing a DCC with an SDCC, including procedures for transferring software configuration parameters from the old DCC to the new SDCC, and setting software parameters (jumpers) on the SDCC for configuration functions performed via hardware jumpers on the DCC.

When replacing a DCC, specify a DS215SDCC as a replacement to ensure that the five memory chips are included.

WARRANTY TERMS

The GE Motors & Industrial Systems Terms and Conditions brochure details product warranty information, including the **warranty period** and **parts and service** coverage.

The brochure is included with customer documentation. It may be obtained separately from the nearest GE Sales Office or authorized GE Sales Representative.

WARRANTY PARTS AND SERVICE

This board has no fuses or other end-user serviceable parts. If it fails, it needs to be replaced as a unit.

To obtain a replacement board, or service assistance, contact the nearest GE Service Office.

Please have the following information ready to exactly identify the **part** and **application**:

- GE requisition or shop order number
- Equipment serial number and model number
- Board number and description

PROCEDURE FOR REPLACING BOARDS

WARNING

To prevent electric shock, turn off power to the drive, then test to verify that no power exists in the board before touching it or any connected circuits.

CAUTION

To prevent equipment damage, do not remove boards or connections, or re-insert them, while power is applied to the drive.

Treat all boards as static-sensitive. Use a grounding strap when changing boards or software chips, and always store boards in anti-static bags or boxes they were shipped in.

To replace an SDCC:

1. **Turn off the power to the drive**, then wait several minutes for all the capacitors to discharge. Test any electrical circuits before touching them to ensure the power is off.

2. Open the drive's cabinet door to access the printed wiring boards. (The DCC or SDCC is located in the drive’s board rack, facing the front.)

3. *If a programmer module is included*, remove the programmer by pulling the snaps (holders, located in each corner) outward to release the programmer cover and keypad, then pulling the programmer loose from the KPPL connector. (The keypad plugs into connector KPPL on the LCC or SLCC.)

NOTE

It may be necessary to remove auxiliary boards mounted on the DCC or SDCC as described in step 5 before disconnecting cables from the DCC or SDCC.

4. Carefully disconnect all cables from the DCC or SDCC (and any auxiliary board mounted on standoffs) as follows:
   - Verify cables are labeled with the correct connector name (as marked on the card) to simplify reconnection.
   - For ribbon cables, grasp each side of the cable connector that mates with the board connector and gently pull the cable connector loose.
   - For cables with pull tabs, carefully pull the tab.

5. Remove any auxiliary boards mounted to the DCC or SDCC by removing the screws (with nylon washers) that secure the board to the standoffs on the DCC or SDCC, then remove the auxiliary board.

CAUTION

Avoid dropping mounting hardware into the unit, which could cause damage.

6. Release the DCC or SDCC from the board rack by pushing back on the plastic snaps (holders), then remove the DCC or SDCC.

CAUTION

Always use the nylon washers when inserting screws into the card to avoid damage to the card.

7. Move all standoffs from the card being replaced to the replacement (new) SDCC as follows:
   a. Remove the screws with nylon washers that secure the standoff to the old card by removing the screws with nylon washers from the back side of the old card.
   b. Insert the screws with nylon washers into the same point on the back of the new SDCC as they were removed from on the old card.
   c. Place standoffs into position on the front side of the new SDCC and tighten the screws with nylon washers to secure the standoffs.

8. Set all configurable items on the replacement (new) SDCC in the exact position as those on the card being replaced.

NOTE

When replacing an SDCC, if a board revision has added or eliminated a configurable component, or re-adjustment is needed, refer to Table 2. If replacing a DCC with an SDCC, refer to the corresponding paragraph under Replacing/Inserting Software.

NOTE

Because of upgrades, boards of different revision levels may not contain identical hardware. However, GE Drive Systems assures compatibility of its replacement boards.

9. Install the new SDCC into the board rack, ensuring that all holders snap into position to secure the SDCC.

10. Reconnect all cables to SDCC as labeled. Ensure that cables are properly seated at both ends.

11. Install auxiliary boards on standoffs (if applicable) with screws (with nylon washers) removed in step 5 and reconnect all cables as labeled. Ensure that cables are properly seated at both ends.

12. If a Programmer module is included, carefully plug the keypad into connector KPPL on the LCC or SLCC and snap the cover into place.

NOTE

After replacing the SDCC in an application with critical analog I/O functions, the gains and offsets may require fine-tuning to compensate for variations in component tolerances between the old card and the new.

HARDWARE ADJUSTMENTS

Most of the jumper selections have been factory set. The test data sheets supplied with each controller (in the drive door pocket) indicate these positions. Table 2 lists and defines the jumpers.

In most applications, all WJ jumpers are factory set to the correct position, and all JP jumpers except JP1 should be in position 1-2 (JP1 should be in position 2-3). Use these settings unless the instructions indicate otherwise. As described previously, ensure that the jumpers on the new card are placed the same as on the old card, unless the instructions indicate otherwise. Refer to Table 2, which lists the default setting first. Figure 3 shows jumper locations.

NOTE

Some of the configuration functions on the DCC using hardware jumpers are implemented on the SDCC via software jumpers (parameters stored in EEPROM). If replacing a DCC with an SDCC, refer to the following section, Replacing/Inserting Software, for information on setting software jumpers on the SDCC to match hardware jumper settings of the old DCC. (Also see Table 10.)

REPLACING/INSERTING SOFTWARE

The SDCC uses a different EEPROM chip than that used on the DCC, and some of the hardware jumpers on the DCC are implemented as software jumpers on the SDCC. Therefore, the procedures for replacing/inserting software differ, depending upon whether a DCC or SDCC is being replaced. The following paragraphs describe the procedures for replacing an SDCC, and for replacing a DCC with an SDCC.

Replacing an SDCC

When replacing an SDCC, transfer the onboard software to the new card as follows:

NOTE

To ensure compatibility of the onboard software with existing equipment, transfer the four EPROMs from the old card to the new as described in steps 1 and 2.

1. Remove one of the four EPROM chips (U11, U12, U22, or U23) from the old card and insert it into the respective socket on the new SDCC.

CAUTION

To prevent damage to memory chips, ensure that chips are properly oriented when inserting them into sockets.

2. Repeat step 1, one chip at a time, for each of the remaining EPROM chips.

3. Remove the EEPROM (U9) chip from the old card and insert it into the respective socket in the new SDCC.

4. If the failure symptoms that caused the card to be replaced still exist, perform the following:

   a. Install new EPROMs and (blank) EEPROM (shipped with the new card if a DS215SDCC).

   b. Program the new EEPROM per the customer software adjustment values using the ST2000 (see GEH-5860), GE Control Systems Toolbox (see GEH-6333), LynxOS Drive Configurator (see GEH-6203), or ST1000 Drive Configuration Tools (see GEH-6341).

Replacing a DCC with an SDCC

When replacing a DCC with an SDCC, the replacement card must be a DS215SDCC to ensure that the five memory chips are included. The configuration data from the old DCC must be loaded into the new SDCC's EEPROM per the procedure in this paragraph.

The EEPROM (U9) used on an SDCC has twice the capacity of that used on a DCC. Therefore, the chip from the DCC cannot be merely transferred to the new card. To maintain the configuration from the DCC, use the ST2000 (see GEH-5860), GE Control System Toolbox (see GEH-6333), or LynxOS Drive Configurator (see GEH-6203) to load the configuration into the EEPROM supplied with the SDCC.

If the ST2000, GE Control System Toolbox, or LynxOS Drive Configurator is not available, read the configuration from the DCC EEPROM into a file as described in the following procedure. This procedure requires a personal computer capable of serial communications with the drive via the COMPL port, and capable of uploading and downloading files.

NOTE

Step 1 of the following procedure can be performed with the DCC EEPROM installed in either the DCC or SDCC. If the DCC EEPROM is installed in an SDCC, fault 396 (EEBADSIZ) will occur. To prevent this fault from interfering with the software upload, set EE.3 to 21.

1. With the original EEPROM installed, upload its configuration to a file by issuing the following serial command to the drive: **^x0-4095<Enter>**

NOTE

If the new EEPROM is totally blank (no programming label attached), parameters EE.2 and EE.3 must be set to 21 using a Programmer before performing step 2.

2. Install the new EEPROM in the SDCC and download the configuration file to the drive.

Table 10 lists and defines DCC hardware jumpers that have been implemented as software jumpers on the SDCC. After the DCC configuration has been loaded into the SDCC EEPROM, refer to Table 10 and change any software jumper settings required to match the hardware jumper settings of the DCC.

NOTE

The following table defines the hardware jumpers on the DCC Drive Control Card that have been implemented as software parameters on the SDCC Drive Control Card. When replacing a DCC with an SDCC, if a DCC hardware jumper listed has been moved from the default position (listed first in the following table), the corresponding software parameter for the SDCC must be changed to the required value using either the ST2000 (see GEH-5860), GE Control System Toolbox (see GEH-6333), or LynxOS Drive Configurator (see GEH-6203).

Table 10. DCC Hardware Jumpers Implemented as SDCC Software Jumpers

DCC Hardware Jumper		Corresponding SDCC Software Jumper	
Name	**Description**	**Name**	**Description**
JP19	Source of DCP encoder #1 up/down signals 1.2 From NTB/3TB E0A 2.3 From the SPC encoder #1	EE.7.0 FBKJPR	Select source of hardware encoder signals for software encoder #1 0.000 From encoder #1 via NTB/3TB or STBA 1.000 From encoder #1 via the SPC card (SDCCG1 only) SDCCG1 allows encoders 0, 1, and 2 to be used simultaneously with no restrictions, unlike the DCC which had latency constraints on software encoder #0. This jumper is used for backward compatibility only. **WARNING** -- prior to revision 2.22, SDCC firmware tied hardware encoder 0 to software encoder 0 and hardware encoder 1 to software encoder 1. Revision 2.22 permits this mode only by setting EE.7.0; the default mode for EE.7.0 now becomes backward compatible with the DCC. Note that hardware encoder #1 is not supported on the SDCCG3; therefore this jumper should not be set.
JP20	Source of encoder #1 up/down signals 1.2 From NTB/3TB E0B 2.3 From the SPC encoder #1	EE.7.0 FBKJPR	See description above.
JP21	Source of encoder #1 marker signal 1.2 From NTB/3TB E0M 2.3 From the SPC encoder #1	EE.7.0 FBKJPR	See description above.
JP31	Destination of motor control processor serial interface 1.2 Enable NTB/3TB half-duplex RS-422 interface 2.3 Enable SPC full-duplex RS-422 interface	EE.572.3 MBERGJ	Hardware configuration jumper: source of receive for MCP serial port 0.000 Enable NTB/3TB half-duplex RS-422 interface 1.000 Enable SPC RS-422 or SPCB fiber-optic interface This jumper must be set for use with the serial encoder or DC2000 K/L frame multi-bridge LAN options. Changes to this jumper only take effect when the drive is stopped. The serial encoder interface is supported only on SDCCG1 cards, and is not available when using SDCCG3 cards.
JP32	Enable NTB/3TB encoder #0 marker input into the encoder processing PAL, U30 1.2 Not Enabled 2.3 Enabled	EE.9.7 CFG2JP	Hardware configuration jumper: enable marker channel for encoder 0 0.000 Not enabled 1.000 Enabled (valid only with SDCCG1 cards) Neither SDCCG3 nor STBA boards support the encoder marker channel. Setting EE.9.7 under these conditions will cause mis-operation of the encoder #0 feedback.

Table 10. DCC Hardware Jumpers Implemented as SDCC Software Jumpers — Continued

DCC Hardware Jumper		Corresponding SDCC Software Jumper	
Name	**Description**	**Name**	**Description**
JP34	Source of signal into DCP's external timer/ counter input 1.2 From NTB/3TB T0IN 2.3 From signal selected by JP23 2.4 Pulled high, NTB/3TB T0OUT timed output mode usage	EE9.0 CFG2JP	Hardware configuration jumper: Source for DCP timer/ counter #0 0.000 Enable T0IN from NTB/3TB board 1.000 Enable ANTC from SDCC card 2.000 Enable free-running internal counter 3.000 Inhibit counting This jumper is not currently used in the AC/DC2000. TC2000 uses setting 2 to use the timer as a free-running counter.

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