Honeywell

Application Module^{X} Service

AX13-510

TotalPlant

2. Application Module^{X}

2.1 A^{X}M Functionality

General introduction

The Application Module^{X} (A^{X}M) provides the functionality of a standard Application Module (AM) coupled with an HP-UX-based coprocessor.

This hardware combination provides the capability for delivering powerful higher level control schemes to the TDC 3000^{X}. It also provides the capability of adapting and utilizing third party control solutions.

Two performance levels of the coprocessor are available. The basic coprocessor operates at 64 MHz and a high performance coprocessor will operate at 100 MHz.

Supports existing AM functionality

The A^{X}M continues to provide the full functionality of the existing Application Modules (AM). This is accomplished by the LCN node processor portion in the A^{X}M

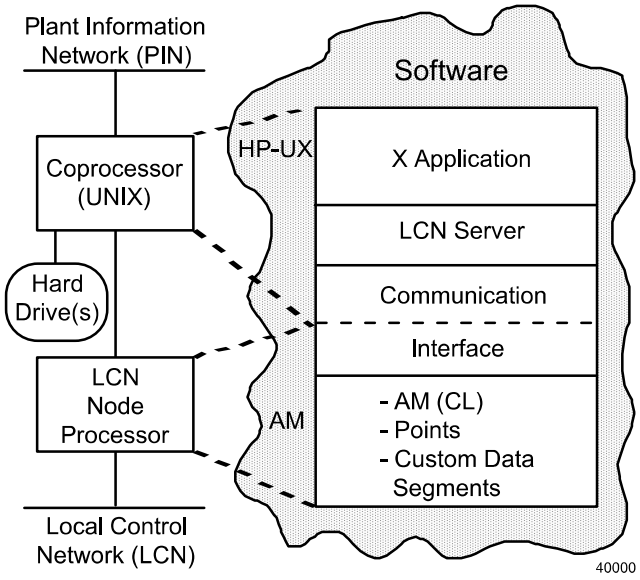
Functionality Diagram

The following diagram illustrates that there are two distinct processors in the A^{X}M node. A standard LCN node processor is coupled to an HP-UX-based coprocessor.

The total A^{X}M software responsibility of both processors is identified by the dotted lines.

Notice that both processors must work through their respective portions of the communication software to successfully pass information between them.

X applications will be executed in the coprocessor. Access to LCN point data is done through the LCN node processor. The Control Language (CL) running in the node processor has been modified to include mechanisms for calling and starting solutions resident in the coprocessor.



2.2 Hardware Organization

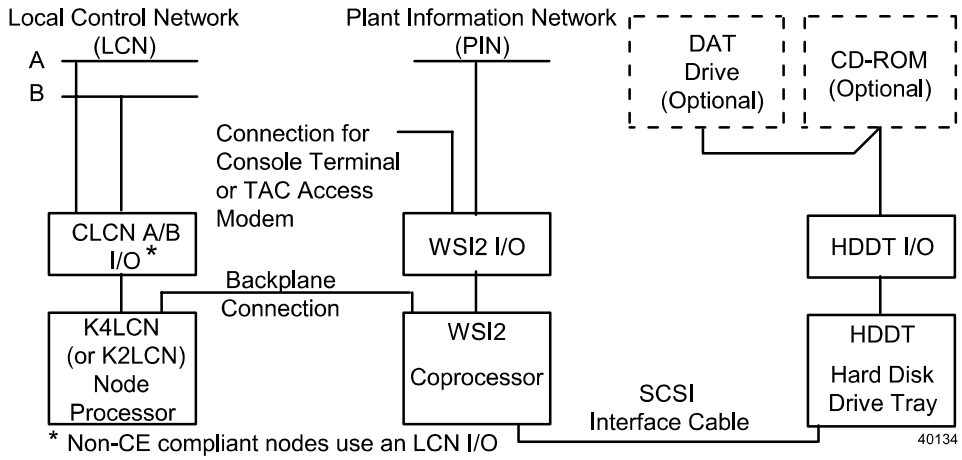
AXM Hardware block diagram

Two versions of A^{X}M hardware will be available. One uses the K2LCN (or K4LCN) board as the LCN node processor and the other uses the HMPU/ LLCN/QMEM combination of boards as the LCN node processor.

The diagrams on the following two pages show the major hardware components that make up the A^{X}M hardware. Pay particular attention to the following:

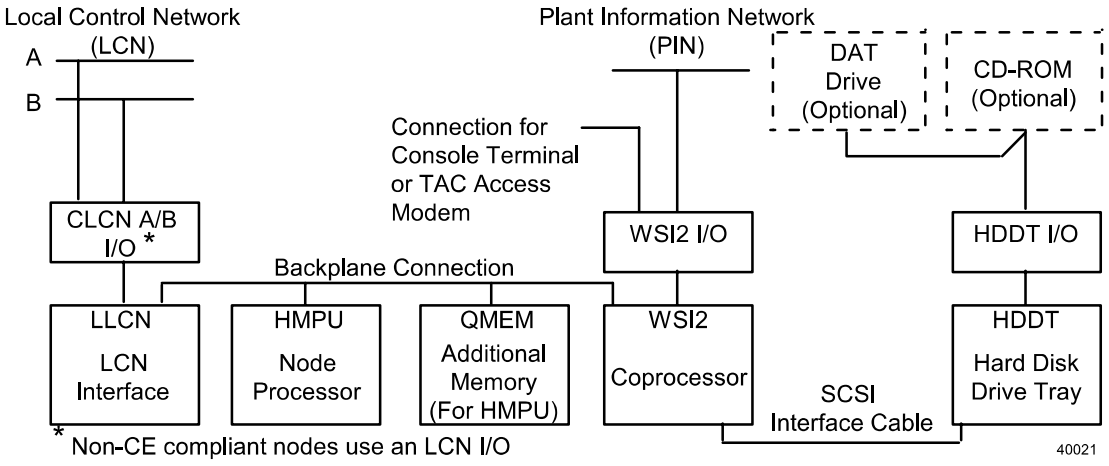
- Names and acronyms of the components
- Interconnection between components
- External connections to:
  - Local Control Network (LCN)
  - Plant Information Network (PIN)
  - "Console terminal" (when required for initial configuration or troubleshooting). A console terminal is a simple keyboard and display device that has no processing capability. Several device types can be used to satisfy this requirement. They are addressed later in this manual.
  - Modem for Technical Assistance Center (TAC) access (if required for complex problem isolation activities).
  - DAT drive (optional) to support hard disk backup, restore, and software update activities. It is also used for recovery activities in the event of some hard disk drive failures.
  - CD-ROM (optional) provides access to the HP-UX online software documentation.

K2LCN/K4LCN hardware version



HMPU hardware version

The following diagram illustrates the HMPU version of hardware.



2.3 Board Slot Definition

Overview of chassis types

The A^XM will appear in two types of LCN node hardware chassis. They are

Five-slot chassis (when using a K2LCN/K4LCN node processor)

Ten-slot chassis (when using an HMPU node processor)—This specific Ten-slot chassis has a split backplane with 6 slots (bottom) dedicated to one LCN node and 4 slots (top) for another LCN node. This Ten-slot chassis has been used in other special LCN applications. A second node in slots 7-10 is not allowed in the case of an A^XM.

Five-Slot board placement

The following tables show the A^XM board placement for the Five-slot chassis using the K4LCN or K2LCN node processor.Two versions of board placement are used depending on the size of the coprocessor memory which is located on the WSI2 board. The 256 megabyte size requires additional space above the WSI2 board.

Table 2-1 Five-Slot Chassis Board Locations (32/64/128 MB Coprocessor Memory Sizes)

Slot	Front	Rear
5	Optional Application Board	
4	Hard Disk Drive Tray (occupies two slots)	
3		HDDT I/O
2	WSI2 *	WSI2 I/O
1	K2LCN-8 or K4LCN-8 (or -16)	CLCN A/B or LCN I/O **

Table 2-2 Five-Slot Chassis Board Locations (with 256 MB Coprocessor Memory)

Slot	Front	Rear
5	Hard Disk Drive Tray (occupies two slots)	
4		HDDT I/O
3	(Space for extra WSI2 Memory) WSI2 *	
2		WSI2 I/O
1	K2LCN-8 or K4LCN-8 (or -16)	CLCN A/B or LCN I/O **

* Two versions of the WSI2 board are available to provide the 64 MHz and 100 MHz coprocessors.

** Non-CE Compliant versions use the LCN I/O.

Ten-slot board placement

The following two tables show the A^{X}M board placement for the 10-slot chassis using the HMPU node processor. Two versions of board placement are used depending on the size of the coprocessor memory which is located on the WSI2 board. The 256 megabyte size requires additional space above the WSI2 board.

Slots 7 through 10 do not share a common backplane for interconnection with slots 1 through 6.

The Hard Drive Disk tray does not depend on the backplane for signal interconnection with other slots. It only uses the slots it occupies to obtain power, which is common to all slots.

Table 2-3 Ten-Slot Chassis Board Locations

Slot	Front	Rear
10	Unusable slot	
9	Unusable slot	
8	Hard Disk Drive Tray	
7	(occupies two slots)	HDDT I/O
6	WSI2 *	WSI2 I/O
5	Optional Application board	
4	Optional memory board	
3	QMEM-4	
2	LLCN	CLCN A/B or LCN I/O **
1	HMPU	

* Two versions of the WSI2 board are available to provide the 64 MHz and 100 MHz coprocessors.

** Non-CE Compliant versions use the LCN I/O.

Table 2-4 Ten-Slot Chassis Board Locations (with 256 MB Coprocessor Memory)

Slot	Front	Rear
10	Unusable slot	
9	Unusable slot	
8	Hard Disk Drive Tray	
7	(occupies two slots)	HDDT I/O
6	(Space for extra WSI2 memory)	
5	WSI2 *	WSI2 I/O
4	Optional Application board	
3	QMEM-4	
2	LLCN	CLCN A/B or LCN I/O **
1	HMPU	

* Two versions of the WSI2 board are available to provide the 64 MHz and 100 MHz coprocessors.

** Non-CE Compliant versions use the LCN I/O.

2.4 Power Supply

Introduction

The A^XM node contains a power supply (55 amp) that is used in many other LCN node types.

It is capable of producing output voltage margins of +5% and -5% that, in some cases, are used in factory test and troubleshooting activities. This margining is controlled by the jumper on the face of the power supply. See the following diagram.

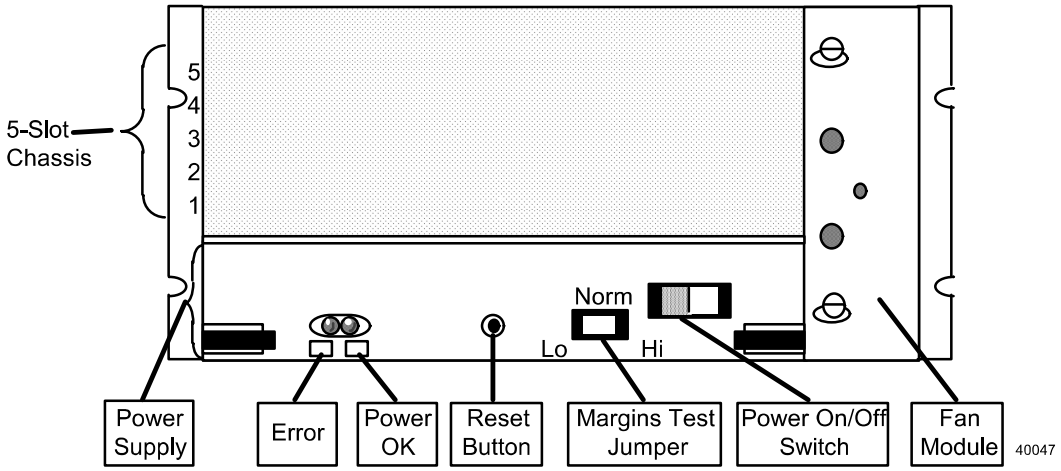
Similar power supplies are used in both the K2LCN/K4LCN (Five-slot) and HMPU (Ten-slot) versions of A^XM.

Node power margin restrictions

> **WARNING**
>
> The low power margin (-5%) must never be used in the A^XM. The coprocessor and hard disk drive design allows for only a -2.5% margin. Using -5% margins will produce unpredictable results.
>
> The high (+5%) power margin can be used by factory test and during troubleshooting activities. Honeywell does not recommend using any power margins while a node is on process.

Node power supply diagram

The following diagram shows the power supply in a Five-slot chassis (K2LCN/K4LCN version). A similar power supply is used in the Ten-slot chassis (HMPU version).



3. Hardware Description of LCN Node Processors

3.1 K2LCN-X Node Processor

Overview

The K2LCN processor board contains all of the essential parts to make up the kernel portion of any LCN node. It includes a 68020 processor, LCN interface circuits, and 6 or 8 megawords of on-board memory (for AXM). It does not have floating point calculation hardware capability. The exact memory size is determined by which option is purchased. A minimum of 6 megawords is required to support R500 software.

Changing memory size requires the replacement of the current K2LCN board with a board containing the proper memory complement. This board cannot be upgraded in the field.

The K2LCN board memory size is easily recognized by the -X portion of the name on the left extraction lever; i.e., K2LCN-6 = 6 megawords or K2LCN-8 = 8 megawords.

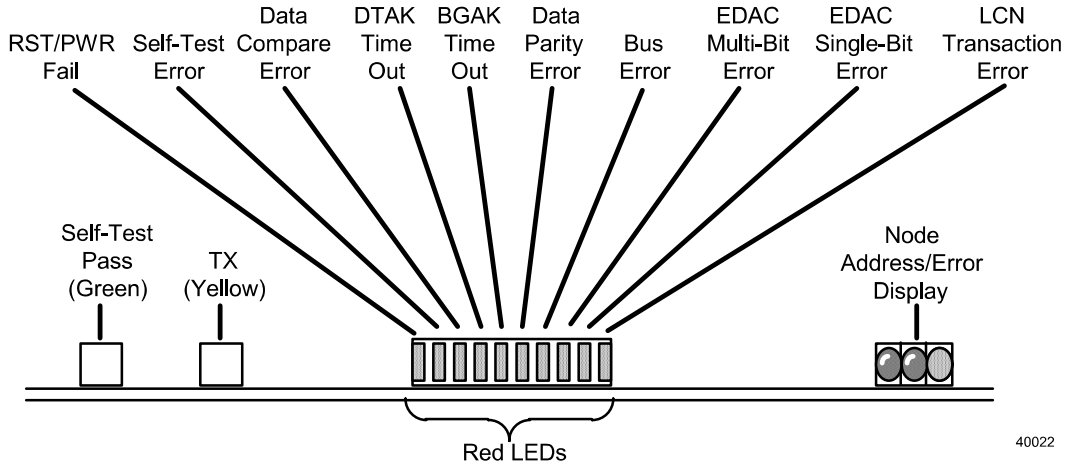
K2LCN indicators

The K2LCN board indicators are visible from thefree edge of the board while the board is installed in a module chassis. The indicators provide a visual indication regarding the present condition of the board.

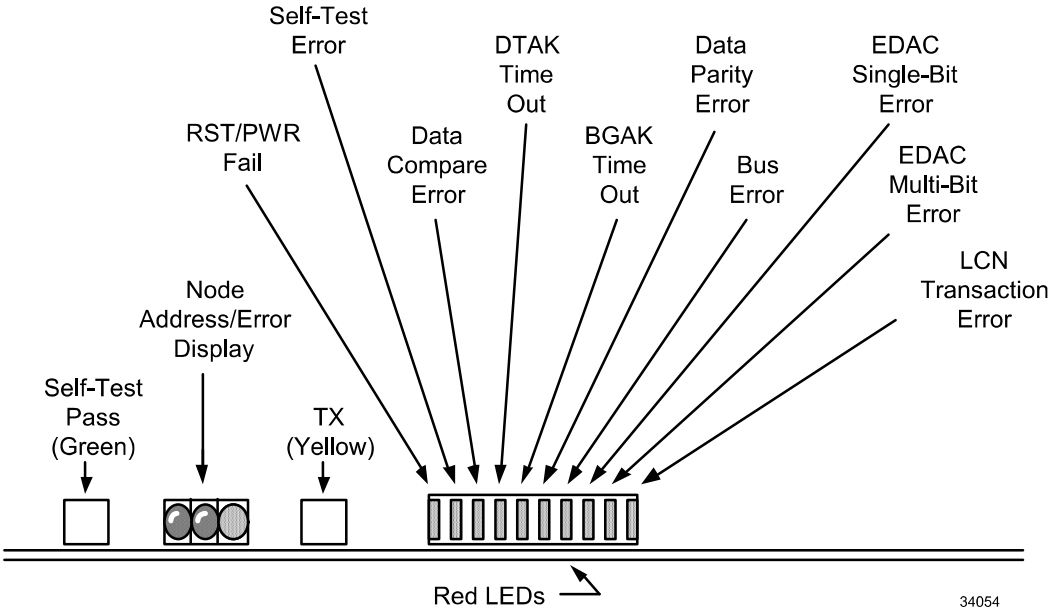
Two illustrations of the indicators follow. The first illustration shows the indicator layout on an early production K2LCN board, assembly 51401551-x00. The second illustration shows the indicators on the latest production K2LCN board, assembly 51402615-x00.

The indicators provide identical information on both boards.

The indicators on the early production K2LCN board, assembly 51401551-x00, are shown in the following illustration.



The indicators on the latest production K2LCN borad, assembly 51402615-x00, are shown in the following illustration.



Indicator description

The following table provides descriptions of the indicators on the K2LCN board. Reference the preceding diagrams.

Table 3-1 K2LCN Board Indicators

LED	Description	Suspected cause if abnormal
Self-Test Pass	On after board passes self-test. Normally on.	K2LCN
TX	On when transmitting on the LCN. Normally on or flashing rapidly.	K2LCN
RST/PWR fail	On when a reset operation caused by the reset button or power on is in progress. Normally off.	K2LCN
Self-Test Error	On to indicate a board self-test error. Normally off.	K2LCN
Data Compare Error	On to indicate an on-board data compare error. Normally off.	K2LCN
DTAK Time Out	On to indicate a Data Transfer Acknowledge failure. Normally off.	K2LCN
BGAK Time Out	On to indicate a Bus Grant Acknowledge failure. Normally off.	K2LCN or other board(s) in chassis
Data Parity Error	On to indicate an on-board data parity error. Normally off.	K2LCN
Bus Error	On to indicate a detected backplane bus parity error. Normally off.	K2LCN, other board(s) in chassis, or backplane
EDAC Single-Bit Error	On to indicate a single-bit (correctable) RAM error. Normally off.	K2LCN
EDAC Multiple-Bit Error	On to indicate a multiple-bit (uncorrectable) RAM error. Normally off.	K2LCN
LCN Transaction Error	On to indicate communication problems with the LCN. Normally off.	K2LCN or CLCN A/B (LCN I/O) or LCN network

K2LCN Pinning

The K2LCN board has an LCN node number pinning feature on the board itself. This feature is duplicated on the CLCN A/B I/O or LCN I/O board that is installed directly behind the K2LCN board in the $A^{X}M$ Five-Slot Module chassis.

ATTENTION

The address pinning jumpers must all be removed from the K2LCN board when it is used in conjunction with an CLCN A/B I/O (or LCN I/O) board. The node number pinning must be done on the CLCN A/B I/O (or LCN I/O) board in this case.

The K2LCN board pinning requirement for the $A^{X}M$ is shownin the following two illustrations.

The first illustration shows the location of the address pinning lbock on the early production K2LCN board, assembly 51401551-x00. The second illustration shows the location of the address pinning block on the latest production K2LCN board, assembly 51402615-x00.