IVCR2403/4/5 24V 4A Peak Source and Sink Dual-Channel Driver

1. Features

- Industry standard SOIC-8 pinout
- Two independent gate drive channels
- 4A source and sink peak drive current
- Wide VDD range up to 24V
- Separated enable inputs
- Two channels in parallel for high current driving (IVCR2403/4)
- Inverting and non-inverting options
- VDD UVLO protection
- TTL and CMOS compatible inputs
- Low propagation delays
- 1ns typical delay matching between two channels (IVCR2403/4)
- Outputs held low when floating inputs
- Operating temperature range -40°C to 125°C

2. Applications

- AC/DC and DC/DC converters
- Server and Telecom rectifiers
- EV/HEV inverters and DC/DC converters
- PV boosters and inverters
- UPS
- Motor Control
- Emerging Wide Band-Gap Power Devices

3. Description

The IVCR2403/4/5 is a 4A dual-channel, high-speed, low-side gate driver, capable of effectively and safely driving MOSFETs and IGBTs. Low propagation delay and mismatch and compact SOIC-8 package enables MOSFETs to switch at hundreds of kHz. It is very suitable for server and telecom power supply's synchronous rectification driving, where synchronous MOSFET's dead time accuracy directly impacts converter's efficiency. The driver is capable to parallel two channels to increase output driving current. The input thresholds are based on TTL with voltage tolerance from -5V to 20V.

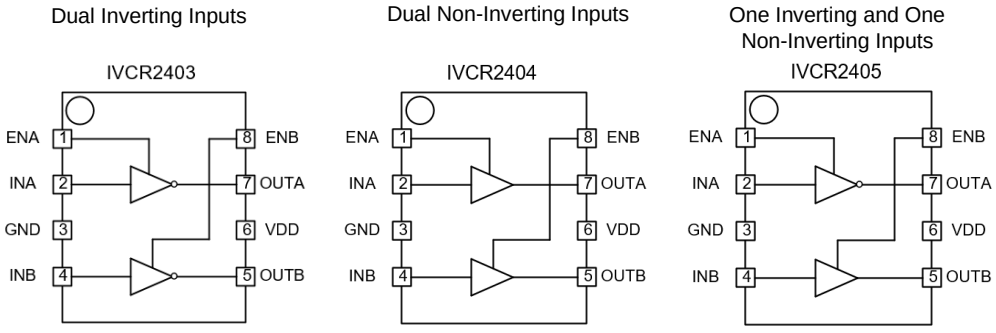
Wide VDD operating range from 4.5V to 20V enables effective driving with MOSFET or GaN power switches. Integrated UVLO protection ensures output held at low under abnormal conditions.

The independent inputs range from -5V to 24V ensure robust operation with undershoot or overshoot induced by parasitic inductances. The input thresholds are compatible with TTL input.

Device Information

PART NUMBER	PACKAGE	PACKING
IVCR2403DR	SOIC-8	Tape and Reel
IVCR2403D	SOIC-8	Tube
IVCR2404DR	SOIC-8	Tape and Reel
IVCR2404D	SOIC-8	Tube
IVCR2405DR	SOIC-8	Tape and Reel
IVCR2405D	SOIC-8	Tube

Pin Configuration



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4. Pin Configuration and Functions

PIN	NAME	I/O	DESCRIPTION
1	ENA	I	Channel A enable input
2	INA	I	Channel A input
3	GND	G	Driver ground
4	INB	I	Channel B input
5	OUTB	O	Channel B driver output
6	VDD	P	Positive bias supply
7	OUTA	O	Channel A driver output
8	ENB	I	Channel B enable input

Truth Table

VDD is higher than UVLO threshold. OUTx (x = A or B) is independently controlled by INx and ENx.

IVCR2403/4/5				IVCR2403		IVCR2404		IVCR2405	
ENA	ENB	INA	INB	OUTA	OUTB	OUTA	OUTB	OUTA	OUTB
H or floating	H or floating	L	L	H	H	L	L	H	L
H or floating	H or floating	L	H	H	L	L	H	H	H
H or floating	H or floating	H	L	L	H	H	L	L	L
H or floating	H or floating	H	H	L	L	H	H	L	H
L	L	X	X	L	L	L	L	L	L
X	X	floating	floating	L	L	L	L	L	L

5. Specifications

5.1 Absolute Maximum Ratings

Over free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
V_{DD}	Total supply voltage (reference to GND)	-0.3	24	V
OUTA, OUTB	Gate driver output voltage	-0.3	V_{DD}+0.3	V
INA, INB	Signal input voltage	-5	24	V
T_J	Junction temperature	-40	150	°C
T_{STG}	Storage temperature	-65	150	°C

(1) Operating beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended period may affect device reliability.

5.2 ESD Rating

		Value	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	+/-2000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	+/-500	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operation Conditions

		MIN	MAX	UNIT
V_{DD}	Supply voltage	4.5	20	V
$V_{INx, ENx}$	Input voltage	0	20	V
T_A	Ambient temperature	-40	125	°C

5.4 Thermal Information

		Value	UNIT
$R_{\theta JA}$	Junction-to-Ambient	128	°C/W
$R_{\theta JB}$	Junction-to-PCB	68.5	°C/W

5.5 Electrical Specifications

Unless otherwise noted, V_{DD} = 12 V, T_A = –40°C to 125°C
Currents are positive into and negative out of the specified terminal. Typical condition specifications are at 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BIAS CURRENT						
I_{DDoff}	Startup current	VDD=3V, OUTA=OUTB=LOW		70		μA
I_{DDq}	Quiescent current	INA=INB=0V		180		μA
UVLO (IVCR2404)						
V_{ON}	Under voltage thresholds	Rising threshold		3.8	4.2	V
V_{OFF}		Falling threshold	3.2	3.5		
UVLO (IVCR2403/5)						
V_{ON}	Under voltage thresholds	Rising threshold		3.8	4.25	V
V_{OFF}		Falling threshold	3.2	3.5		
INVERTING INPUT (INA, INB of IVCR2403 and INA of IVCR2405)						
V_{INH}	Input rising threshold			1.8	2.4	V
V_{INL}	Input falling threshold		0.8	1.1		V
V_{INHYS}	Input hysteresis			0.8		V
V_{INNS}	Input negative voltage capability		-5			V
NON-INVERTING INPUT (INA, INB of IVCR2404 and INB of IVCR2405)						
V_{INH}	Input rising threshold			2.0	2.4	V
V_{INL}	Input falling threshold		0.8	1.2		V
V_{INHYS}	Input hysteresis			0.8		V
V_{INNS}	Input negative voltage capability		-5			V
ENABLE INPUT (ENA, ENB)						
V_{ENH}	Enable input rising threshold			1.8	2.2	V
V_{ENL}	Enable input signal threshold		0.8	1.1		V
V_{INHYS}	Enable input hysteresis			0.7		V
OUTPUTS (OUTA, OUTB)						
I_O	Peak source and sink currents	C_{LOAD} = 0.22uF, with external current limiting resistors, 1kHz switching frequency		4		A
V_{OH}	Output high voltage	I_{OUTH} = -10mA		V_{DD}-0.05	V_{DD}-0.12	V
V_{OL}	Output low voltage	I_{OUTL} = 10mA		0.0057	0.012	V
R_{OH}	Output static pull-up resistance			5	12	Ω
R_{OL}	Output pull-down resistance			0.57	1.2	Ω
Timing						
TD_r	Output rising delay	C_{LOAD} = 1.8nF		16		ns
TD_f	Output falling delay			16		
T_r	Rise time	C_{LOAD} = 1.8nF		6		ns
T_f	Fall time			6		
T_{dm}	Delay mismatch	INA=INB, ENA=ENB=VDD (IVCR2403 and IVCR2404)		1		ns

6. Typical Characteristics

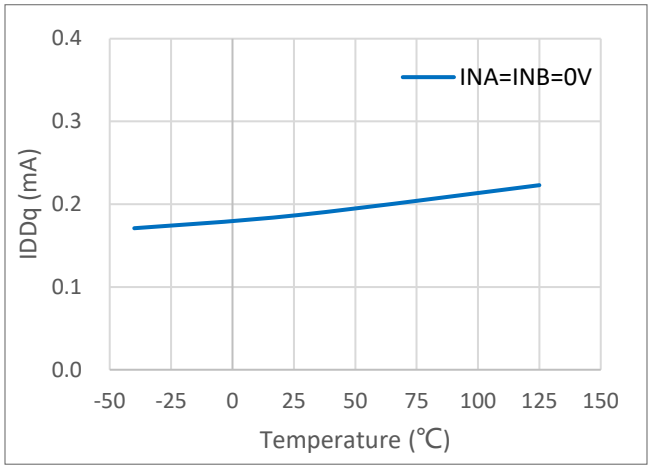


Figure 1. Quiescent Current IDDq vs Temperature

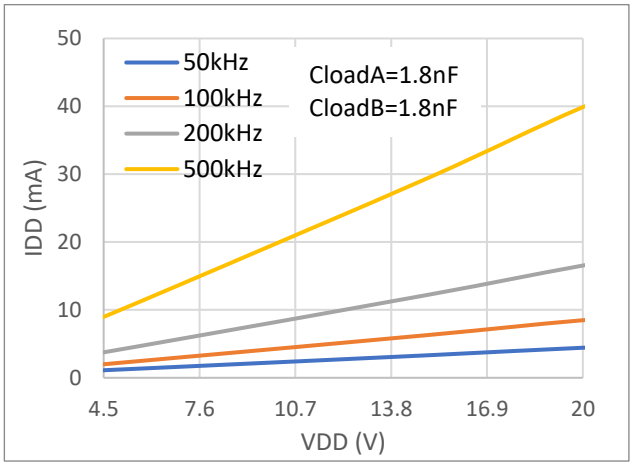


Figure 2. Operating Current IDD vs VDD

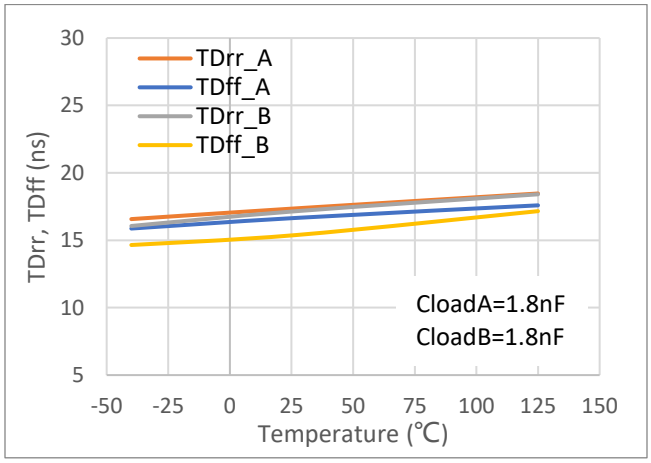


Figure 3. Propagation Delay vs Temperature

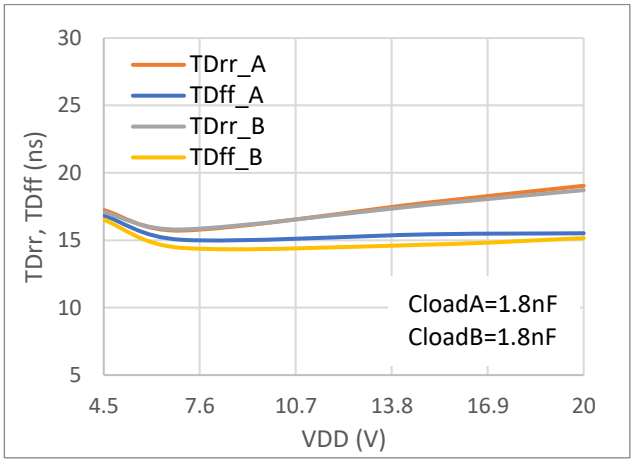


Figure 4. Propagation Delay vs VDD

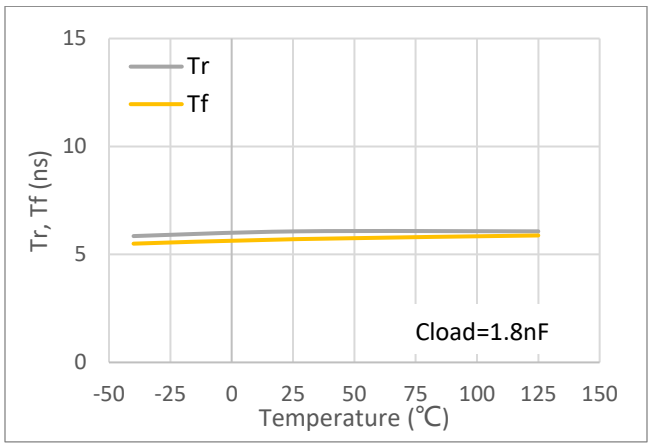


Figure 5. Rise Time and Fall time vs Temperature

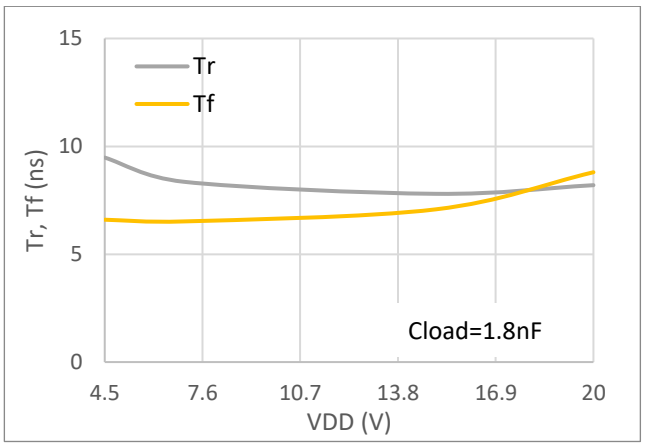


Figure 6. Rise Time and Fall time vs VDD

7. Detail Descriptions

IVCR2403/4/5 driver provides dual-channel high-speed low-side gate drive. IVCR2403/4 features tight mismatching outputs when two channels are paralleled to drive large or paralleled power switches.

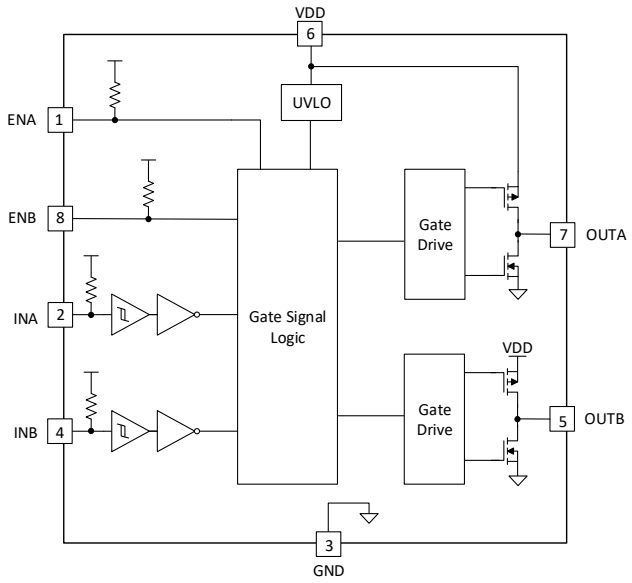


Figure 7. IVCR2403 Block Diagram

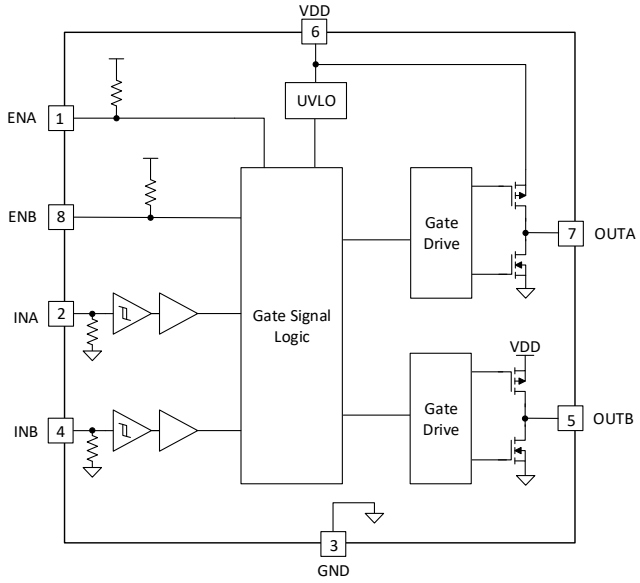


Figure 8. IVCR2404 Block Diagram

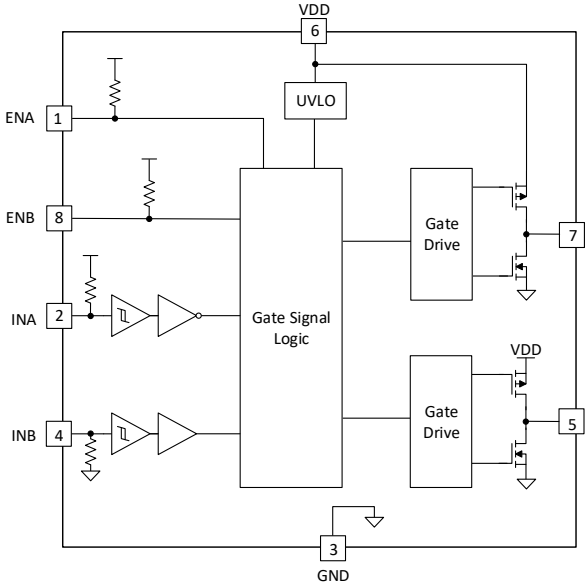


Figure 9. IVCR2405 Block Diagram

7.1 Input Signals INA and INB

INA and INB are gate driver inputs. The pin has a pullup resistor on all the inverting inputs (INA, INB of IVCR2403 and INA of IVCR2405) and has a pulldown resistor on all the non-inverting inputs (INA, INB of IVCR2404 and INB of IVCR2405). When left floating, outputs are pulled to GND. The input is a TTL and CMOS compatible logic level with maximum 24V input tolerance.

7.2 Enable Signals ENA and ENB

ENA and ENB are enable control signals. The enable control signal is a TTL and CMOS compatible logic level with maximum 24V tolerance. When ENx is driven low the OUTx is pulled to GND. When ENx is driven high or left floating, the OUTx follows INx (INA, INB of IVCR2404 and INB of IVCR2405) or is the inverting of INx (INA, INB of IVCR2403 and INA of IVCR2405). The enable pins have a weak pullup.

7.3 OUTA and OUTB

OUTA and OUTB are totem-pole outputs, which consist of a hybrid pullup and an N-channel MOSFET for pulldown. Each output stage in IVCR2403/4/5 can supply 4A peak source and 4A peak sink current pulses. The output voltage swings between VDD and GND providing rail-to-rail operation. The presence of the MOSFET body diodes also offer voltage clamping paths to limit overshoot and undershoot. That means that in many cases, external Schottky diode clamps may not be necessary.

7.4 VDD and Under Voltage Protection

IVCR2403/4/5 maximum voltage rating is 24V. It is suitable for Si MOSFET, IGBT and SiC MOSFET gate drive. The driver has internal under voltage lockout (UVLO) protection feature. When VDD level is below UVLO threshold, this circuit holds the output LOW, regardless of the status of the inputs.

8. Application Implementation

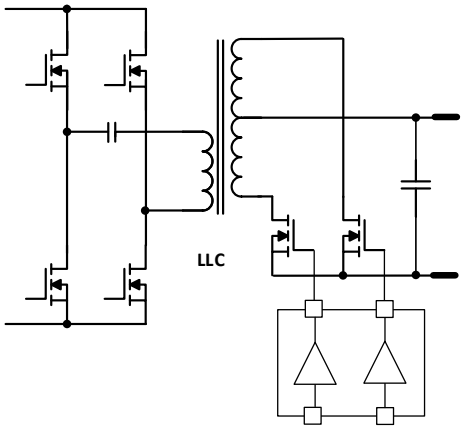


Figure 10. Two channels driven separately (IVCR2403/4/5)

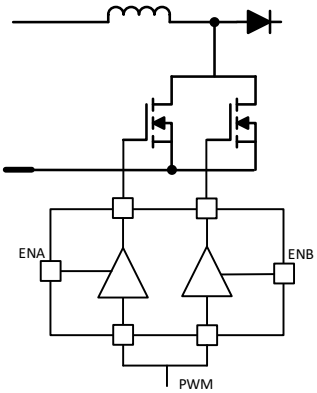


Figure 11. Two paralleled switches driver by two outputs with minimized mismatch (IVCR2403/4)

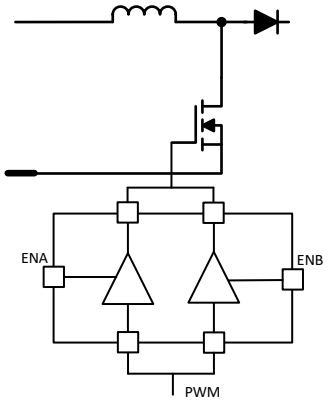


Figure 12. A large switch driver by two paralleled outputs with minimized mismatch (IVCR2403/4)

9. Layout

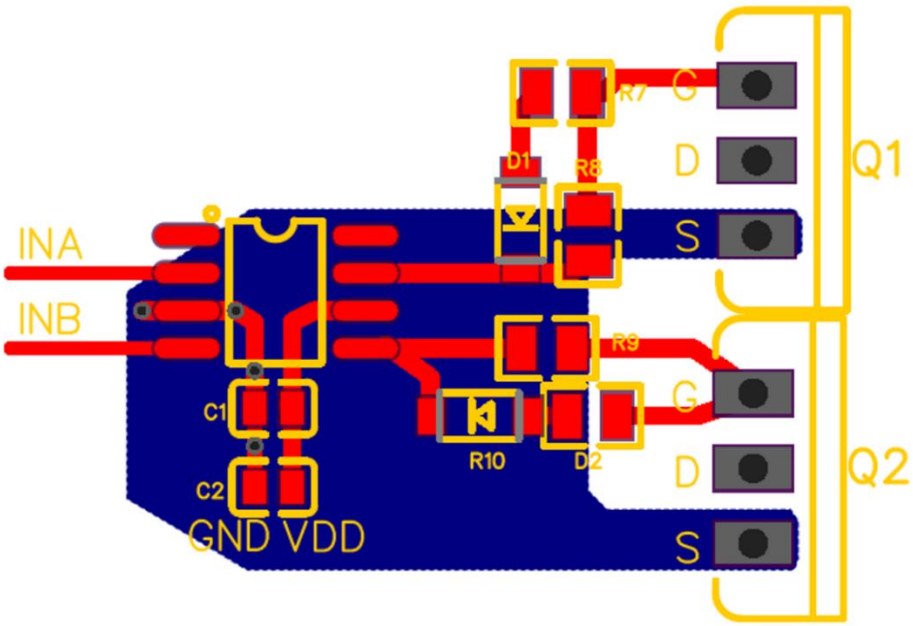
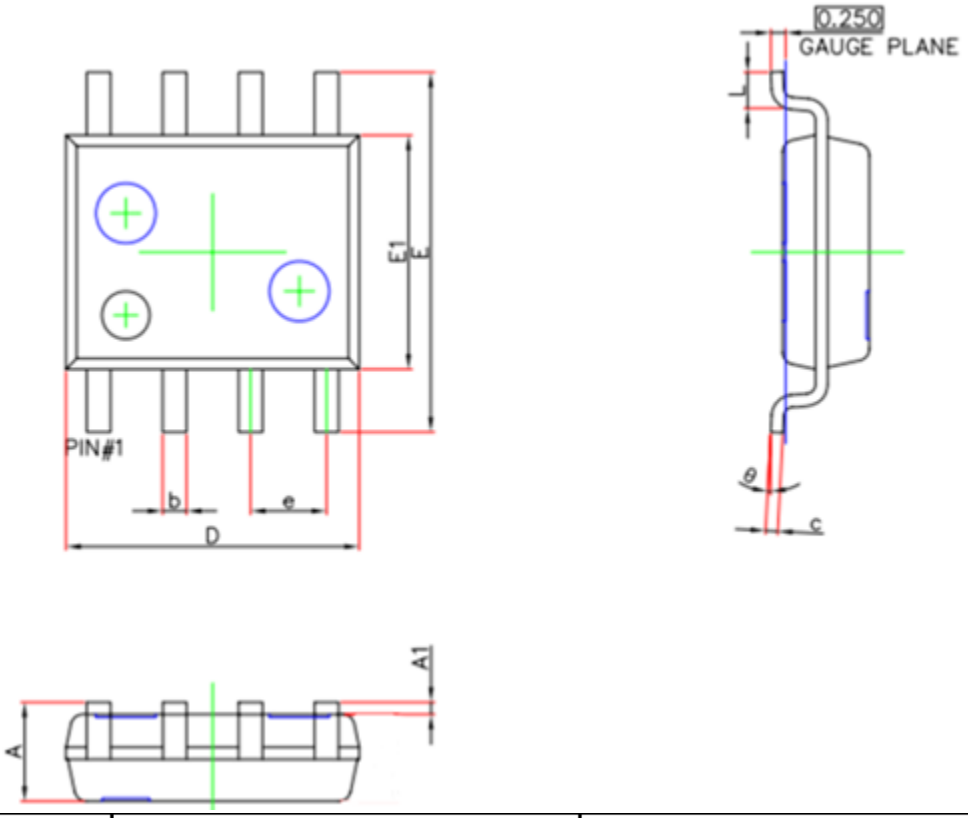


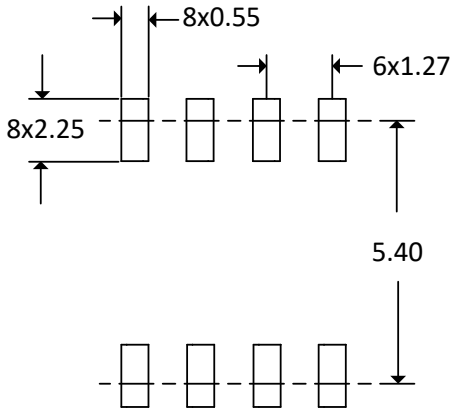
Figure 13. Layout Example for IVCR2403/4/5

10. Package Information

SOIC-8 Package Dimensions



Symbol	Dimensions in Millimeters		Dimensions in Inches	
	Min.	Max.	Min.	Max.
A	1.350	1.750	0.053	0.069
A1	0.110	0.250	0.004	0.010
b	0.310	0.510	0.012	0.020
c	0.130	0.250	0.005	0.010
D	4.810	5.000	0.189	0.197
E	5.800	6.190	0.228	0.244
E1	3.810	3.980	0.150	0.157
e	1.270		0.050	
L	0.410	1.270	0.016	0.050
θ	0°	8°	0°	8°



SOIC-8 Recommended Soldering Dimensions